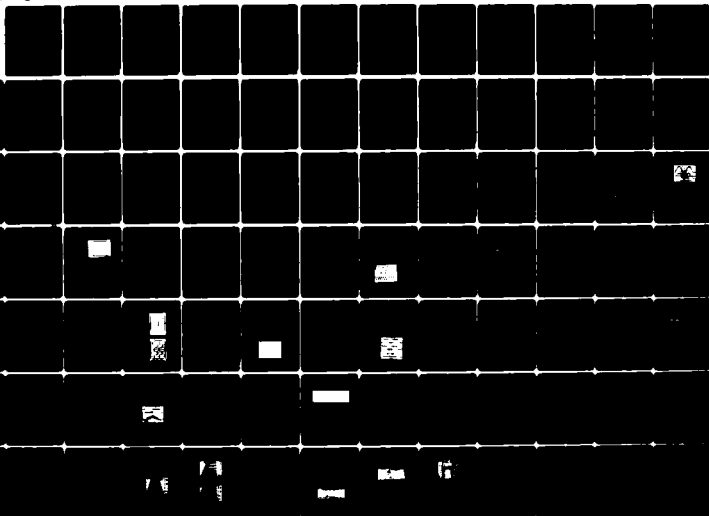


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A CCD MONOLITHIC LMS ADAPTIVE ANALOG SIGNAL PROCESSOR INTEGRATE--ETC(U)
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**A CCD MONOLITHIC LMS ADAPTIVE ANALOG SIGNAL
PROCESSOR INTEGRATED CIRCUIT**

FINAL REPORT

Contract No. N00173-77-C-0328

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TABLE OF CONTENTS

	<u>Page</u>
Acknowledgements	iv
Abstract	vi
I. INTRODUCTION	1-1
II LMS ERROR ALGORITHM	2-1
Adaptive Filter: Direct Technique	2-3
Adaptive Filter: LMS Algorithm Approach	2-6
LMS Clipped Data: Algorithm Characteristics	2-13
III. CCD MONOLITHIC ADAPTIVE SIGNAL PROCESSOR	3-1
Adaptive Filter Generalized Block Diagram	3-1
Description of Basic Components	3-6
Chip Timing and Clock Generation Circuitry	3-42
Features of the Monolithic Adaptive Filter	3-47
IV. FABRICATION TECHNOLOGY	4-1
V. APPLICATIONS	5-1
Adaptive Noise Canellation	5-1
Adaptive Linear Prediction for Narrowband Speech/ Voice Processing	5-6
Adaptive Echo Cancellation Filters	5-10
System Modeling	5-12
VI. CONCLUSIONS	6-1
Appendix A	A-1

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ABSTRACT

This report describes the implementation of a recursive, stochastic, algorithm, the Least-Mean-Square (LMS) Error algorithm, in a 16-tap weight CCD monolithic analog adaptive filter with electrically-reprogrammable MOS analog conductance weights. The analog and digital peripheral MOS on-chip circuits are provided with CMOS technology.

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I. INTRODUCTION

The recommendation of an early study program¹ was to examine the possibility of electrically reprogrammable analog weights at tap positions along a CCD analog delay line in order to form a basic linear combiner for adaptive filtering. A step was taken in this direction with the development of a serial in/parallel out (SI/PO) CCD² with a floating clock electrode circuit for the attachment of conductance weights.³ The latter circuit combined the advantages of MOS and bipolar technologies⁴ to sense non-destructively the signal charge under a floating gate electrode in the form of displacement charge stored on a MOS transistor amplifier.⁵

¹ M.H. White and W.R. Webb, "Study of the Use of Charge-Coupled Devices in Analog Signal Processing Systems", Final Report, N00014-74-C-0069, May 1974.

² M.H. White, I.A. Mack, F.J. Kub, and D.R. Lampe, "Charge-Coupled Device Analog Signal Processing", Final Report N00014-75-C-0283, Feb. 1976.

³ M.H. White, I.A. Mack, F.J. Kub, D.R. Lampe, and J.L. Fagan, "An Analog CCD Transversal Filter with Floating Clock Electrode Sensor and Variable Tap Gains", ISSCC Technical Digest (1976), p. 194, Philadelphia, Pa.

⁴ F.J. Kub, M.H. White, D.R. Lampe, J.L. Fagan, and I.A. Mack, "CCD/Bipolar Monolithic IC Technology", Abstract #107, p. 207 Extended Abstracts, Vol. 76-1, Electrochemical Society, Spring Meeting, May 2-7, 1976. Washington, D.C.

⁵ I.A. Mack, M.H. White, F.J. Kub, D.R. Lampe, and J.L. Fagan, "A Versatile CCD Analog Transversal Filter with Floating Clock Electrode Sensors", NAECON 76, Dayton, Ohio. May 1976.

The concept of electrically reprogrammable analog conductance weights was introduced with the use of non-volatile MNOS memory transistors biased in their triode regions.⁶⁻⁷ The intent of this approach was to realize adaptive filters based on the least-mean-square (LMS) error algorithm⁸ to optimize the weights and provide storage of the weights for several minutes or longer based upon some anticipated applications.⁹ In addition, many applications required a large number of tap weights which placed severe limitations on the use of multiplying digital-to-analog converters (MDAC's)¹⁰ at each tap site¹¹ or in a multiplexed manner.¹²

⁶ M.H. White, D.R. Lampe, J.L. Fagan, "CCD and MNOS Devices for Programmable Analog Signal Processing and Digital Non-volatile Memory", IEDM Technical Digest (1973), Dec. 1973, p. 130-3.

⁷ D.R. Lampe, M.H. White, J.H. Mims, and G.A. Gilmour, "CCD's for Discrete Analog Signal Processing", INTERCON 74, March 1974, New York City.

⁸ B. Widrow, "Adaptive Filters I: Fundamentals" Rept. SEL-66-126 (TR No. 6764-6) Stanford Electronics Labs (Stanford, Calif.) Dec. 1966.

⁹ M.M. Sondhi and A.J. Presti, "A Self-Adaptive Echo Canceller", B.S.T.J., 1851 (1966).

¹⁰ J.L. McCreary and P.R. Gray, "All MOS Charge Redistribution Analog-to-Digital Conversion Techniques-Part I", IEEE J. of Solid State Circuits, SC-10, 371 (1975).

¹¹ Y.A. Haque and M.A. Copeland, "Design and Characterization of a Real-Time Correlator", IEEE J. of Solid-State Circuits, SC-12, 642 (1977).

¹² C.F. Cowan and J. Mavor, "Noise Cancellation and Inverse Filtering Using a Compact High-Performance CCD Adaptive Filter", Electronics Letters, 15, 35 (1979).

Our experience with MNOS memory transistors¹³ for over a decade, since 1965, and the long-term endurance of these devices to cycling,¹⁴ made the non-volatile transistor a logical selection for a long-term analog storage element with multiplying capabilities. In addition, we had worked on the combination of CCD and MNOS technologies to achieve a monolithic charge-addressed memory cell.¹⁵ Thus, we constructed a 2-tap weight, hybrid, CCD adaptive filter based upon the use of non-volatile MNOS memory transistors as the analog convolver-type weights.¹⁶⁻¹⁸ The results of these studies indicated the feasibility of constructing a monolithic CCD adaptive filter based on the LMS error algorithm. During the study of the 2-tap weight CCD adaptive filter, we realized the difficulty in obtaining uniform MNOS analog characteristics and the requirement for a number of accurate analog programming voltages to adjust the device threshold voltage. These difficulties off-set the long-term storage assets of the MNOS memory transistor and we focused on a new concept for the monolithic implementation

¹³ M.H. White and J.R. Cricchi, "Characterization of Thin-Oxide MNOS Memory Transistors", IEEE Trans. Electron Devices, ED-19, 2380 (1972).

¹⁴ M.H. White, J.W. Dzimianski and M.C. Peckerar, "Endurance of Thin-Oxide Nonvolatile MNOS Memory Transistors", IEEE Trans. Electron Devices, ED-24, 577 (1977).

¹⁵ M.H. White, D.R. Lampe, J.L. Fagan, F. J. Kub, and D.A. Barth, "A Nonvolatile Charge Addressed Memory (NOVCAM) Cell", IEEE J. of Solid-State Circuits, SC-10, 281 (1975).

¹⁶ M.H. White, K. Petrosky, I.A. Mack, L. Lewis, "Adaptive CCD Signal Processing for Sonar Applications", 1977 Int'l Symp. on Circuits and Systems, April 25, 1977, Phoenix, Arizona.

¹⁷ M.H. White, I.A. Mack, L.L. Lewis, G.M. Borsuk, "CCD Adaptive Discrete Analog Signal Processing", Final Report, N000173-76-C-0147, July 1977.

¹⁸ M.H. White, I.A. Mack, G.M. Borsuk, D.R. Lampe, F.J. Kub, "Charge-Coupled Device (CCD) Adaptive Discrete Analog Signal Processing", IEEE J. of Solid-State Circuits, SC-14, 132 (1979).

of programmable analog conductance weights, namely, the bi-directional, charge-control, technique which employs a single-stage CCD structure with each programmable MOS analog conductance. The storage and accumulation of weight values is accomplished with the capacitance associated with each MOS transistor, and is therefore limited by the thermal leakage currents; however, the technique is readily integratable on a monolithic chip and the weight values may be dynamically refreshed once they are optimized, if long-term storage is required in some applications.

This report is a summary of the work performed to realize a 16-tap, CCD Adaptive Analog Signal Processor which uses the LMS Algorithm and is implemented as a monolithic integrated circuit with CMOS technology. The report begins with a historical perspective of the LMS algorithm, followed by a discussion of the monolithic implementation of the LMS Adaptive Signal Processor, and a description of the fabrication technology, applications of the chip, and a final section of conclusions. This development of a CCD Adaptive Analog Signal Processor is the first implementation of such a structure in the form of low cost, low power, integrated circuits with attendant high performance and reliability. This structure may be "pictured" as a smart microprocessor in which the internal parameters (weights) are continuously changed or up-dated to optimize a system performance index.

II. LMS ERROR ALGORITHM

The history of adaptive signal processing might well begin with the introduction of least squares estimation theory by Gauss¹ and Legendre². Gauss introduced this technique to solve a large number of redundant equations and extract the "most probable values" of certain astronomical parameters. Modern adaptive filter theory began with the work of Kolmogorov³ and Wiener⁴ on the prediction and filtering of stationary time series. The Wiener/Kolmogorov work provided the basic design criteria for optimal linear filters to suppress noise, perform signal prediction, and smooth statistically stationary signals. The design of these filters for known statistics is well understood⁵, but practical considerations places limits on the implementation of such filters. Kalman and Bucy⁶ extended the Wiener work to consider the design of time-varying filters for nonstationary signals. In general,

¹K.G. Gauss, Theory of Motion of the Heavenly Bodies, Dover, New York (1963).

²H.W. Sorenson, "Least-Squares Estimation: from Gauss to Kalman", IEEE Spectrum, p. 63, July 1970.

³A. Kolmogorov, "Interpolation and Extrapolation von Stationaren Zufalligen Folgen," Bull Acad. Sci., USSR, Ser. Math., 5, 3 (1941).

⁴N. Wiener, The Extrapolation, Interpolation and Smoothing of Stationary Time Series, Cambridge, Mass, MIT Press (1949).

⁵Y.W. Lee, Statistical Theory of Communication, John Wiley & Sons, New York (1960).

⁶R. Kalman and R. Bucy, "New Results in Linear Filtering and Prediction Theory", Trans. ASME (Ser. D) J. Basic Eng., 83, 95 (1961).

these types of filters have parameters whose values are determined by apriori information on the signal statistics. The so-called Kalman filter represents essentially a recursive solution of Gauss's original least-square problem in which the computational benefits of modern digital computers are used to advantage.⁷

Adaptive filters are a class of "learning machines" in which the filter design (i.e., weight or parameter adjustments) is self-learning and based upon estimated (measured) statistical characteristics of the input and output signals. Adaptive filtering based on a recursive algorithm (correlation-cancellation loop CCL) was employed in the RF antenna field in the 1950's.⁸ Two groups working independently, developed techniques for adaptive interference or clutter cancelling. One group worked on radar IF sidelobe clutter cancellers⁹ with optimization achieved by an algorithm that maximized a generalized signal-to-noise (SNR) ratio.¹⁰ The other group worked on a self-optimizing array for control systems based on sampled signals and a least-mean-square (LMS) error algorithm.¹¹ These two adaptive algorithms, although arrived at with different approaches and different objectives, are nevertheless very similar since they both derive their adaptive parameter adjustments by sensing the correlation between

⁷ A.G. Carlton and J.W. Follin, "Recent Developments in Fixed and Adaptive Filtering", AGARDograph, No. 21 (1956).

⁸ W.F. Gabriel, "Adaptive Arrays-An Introduction", Proc. IEEE, 64 239 (1976).

⁹ P.W. Howells, "Intermediate Frequency Side-Lobe Canceller" U.S. Patent #3, 202, 990 Issued Aug. 24, 1965 (Filed May 4, 1959).

¹⁰ S.P. Applebaum, "Adaptive Arrays", Syracuse University Res. Corp. Rep. SPL, TR 66-1, Aug. 1966.

¹¹ B. Widrow, "Adaptive Filters I: Fundamentals", Standard University, Tech. Rept. N. 6764-6, Dec. 1966.

element signals. Thus, both algorithms use the covariance matrix of the set of system inputs and both converge toward the optimum Wiener solution. In this report, we use the LMS error adaptive algorithm developed by Widrow and Hoff of Stanford University¹² in 1959. Widrow, in a recent survey and tutorial article on adaptive noise cancelling¹³, describes the work performed during the 1960's by he and his colleagues at Stanford.

The adaptive filter operates without apriori knowledge of the signal statistics and the filter uses the available data to design an appropriate filter. The general form of an adaptive filter is limited by practical considerations since the inversion and storage of large matrices of data requires a sizeable volume of computer space and real-time signal processing is difficult to accomplish. The iterative LMS error algorithm of Widrow and Hoff¹² requires very little computer time for memory and the algorithm is suitable for real-time processing of large amounts of data. With this algorithm, the statistics of the signals are not measured explicitly to design the filter, but with a recursive algorithm, the weights are adjusted automatically with the arrival of each new data sample.

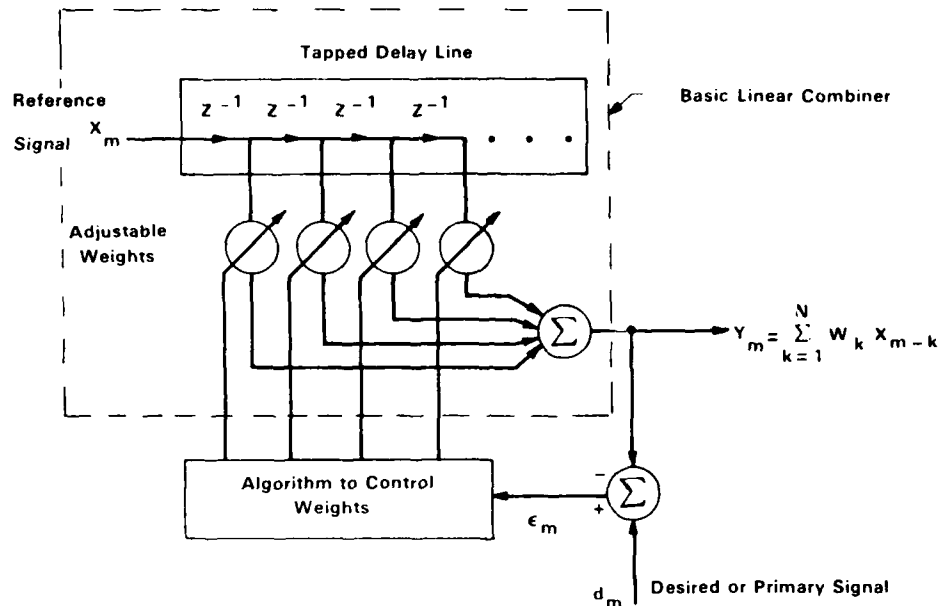
ADAPTIVE FILTER: DIRECT TECHNIQUE

In order to appreciate the degree of computation required in the direct approach to the solution of the least-square-estimation problem, consider the adaptive filter shown in figure 1. We treat the adaptive system as a discrete-time system with the instantaneous error

$$e_m = d_m - y_m \quad (1)$$

¹²B. Widrow and M. Hoff, Jr., "Adaptive Switching Circuits", IRE WESCON, Conv. Rec. Pt. 4, 96 (1960).

¹³B. Widrow, et. al., "Adaptive Noise Cancelling: Principles and Applications", Proc. IEEE, 63, 1692 (1975).



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Figure 1. Adaptive Filter Block Diagram

where d_m is the so-called desired or primary signal, and y_m is the filter output represented by the convolution of the tap weights and the data samples in the delay line,

$$y_m = \sum_{k=1}^N W_k x_{m-k} = W^T X_m \quad (2)$$

where W^T is the transpose of the weight vector and x_m is the data vector. Combining equations (1) and (2) we can form the expectation value of the mean-squared-error (MSE),

$$E(e_m^2) = E(d_m^2) - 2P^T W + W^T R W \quad (3)$$

where $P = E(d_m x_{m-k})$ is the steering vector which describes a cross-correlation between the desired response and the input reference data signal, and $R = E(x_{m-n} x_{m-k})$ is the input covariance matrix describing the statistical properties of the reference signal. The important feature of equation (3) is the MSE is a

quadratic function of the weights and may be considered as a concave hyperboloidal surface in N-dimensions, where N = number of weights. The process of weight adjustment is to minimize the MSE and this involves descending along the hyperboloidal surface to reach the so-called "bottom of the bowl". A popular method to descend along this surface is the gradient technique,

$$\nabla_w E(e_m^2) = -2P + 2RW \quad (4)$$

and the optimum weight vector, generally called the Weiner Weight Vector, is obtained by setting the gradient to zero,

$$W_{opt.} = R^{-1}P \quad (5)$$

and the minimum MSE is obtained with the substitution of equation (5) into (3) to yield,

$$\min E(e_m^2) = E(d_m^2) - W_{opt.}^T P \quad (6)$$

The conventional approach used to solve for the optimum weights involves a two-step process computing and updating the sample covariance matrix with a block of data and then solving equation (5). In order to accomplish this computation, various numerical algorithms have been investigated such as triangularization¹⁴, Levinson-Robinson¹⁵, Householder-transformation¹⁶, and

¹⁴B.S. Atal and S.L. Hanauer, "Speech Analysis and Synthesis by Linear Prediction of the Speech Wave", J. Acoustical Soc. Am., 50, 637 (1971).

¹⁵J.D. Markel, "Digital Inverse Filtering-A New Tool for Formant Trajectory Estimation", IEEE Trans. Audio and Electroacoustics, Au-20, 129 (1972).

¹⁶J. Rogers, "Digital Inverse Filtering of the Speech Waveform", Proc. British Acoust. Soc., 2, Spring Meeting, April 1973.

Gaussian elimination.¹⁷ These methods, even the most efficient one, require a considerable amount of hardware for real-time operation¹⁸⁻¹⁹. The size and power dissipation, in addition to the cost factor, is a principle liability in the so-called direct approach to solving equation (5).

The applications of the adaptive filter are quite broad and perhaps it is fair to classify this device as an adaptive signal processor. The selection of the reference and desired signals in figure 1 determines the particular class of applications. For example, if d_m were derived from the input reference signal to the filter, then we would have an adaptive linear predictor.²⁰ A second example is to use d_m for a signal contaminated with narrow-band noise while the reference input has only the contaminating noise, thereby realizing an adaptive noise canceller.²¹

ADAPTIVE FILTER: LMS ALGORITHM APPROACH

An alternative approach to the direct technique is to use a well-known recursive stochastic algorithm known as the least-mean-square (LMS) error adaptive algorithm.¹² The LMS error algorithm is a practical technique for determining in real-time the optimal weights of the linear combiner in figure 1, which minimizes

¹⁷ J.R. Welch and J.D. Oetting, "Formant Extraction Hardware Using Adaptive Linear Predictive Coding", Proc. Nat'l Telecom Conf., November 1973.

¹⁸ J.G. Dunn, "An Experimental Gigabit/Sec Voice Digitizer Employing Adaptive Prediction", IEEE Trans. on Comp. Tech., Com-19, 1021 (1972).

¹⁹ Voice Processor LSI/Organization Optimization Study, S.E. Hutchings, et. al., TRW Systems, Final Report Contract No. DCA 100-75-C-0020, September 1975.

²⁰ G.S. Kang, "Application of Linear Prediction Encoding to a Narrowband Voice Digitizer", Naval Research Lab. Report 7774, October 31, 1974.

²¹ B. Widrow, et. al., "Adaptive Noise Cancelling: Principles and Applications", Proc. IEEE, 63, 1692 (1975).

the MSE. The important features of the algorithmic approach to the solution of equation (5) are, (1) no explicit measurement of correlation functions, (2) no large memory storage or matrix inversion, and (3) the accuracy is determined by the statistical sample size. These advantages permit an adaptive analog signal processor to be realized as a monolithic integrated circuit.

The minimum of the MSE is found by solving equation (4) with the method of steepest descent. The weight adjustment of the linear combiner is performed in a direction proportional to the negative of this gradient expression. The difference equation which describes this process in real time is given as,

$$w_k(m+1) = w_k(m) - \mu \nabla_{w_k} E(e_m^2) \quad (7)$$

where μ is a factor which is responsible for the stability and rate of convergence of the filter. Combining equations (1) - (4) and (7) we can write

$$w_k(m+1) = w_k(m) + 2\mu E(e_m x_{m-k}) \quad (8)$$

for the k^{th} tap. This expression shows that the incremental weight update is a cross-correlation between the error sequence and the input reference data sequence. The concept is described by a cross-correlation function ρ_k for the k^{th} tap position:

$$\rho_k = \frac{1}{M} \sum_{m=1}^M e_m x_{m-k} \quad (9)$$

over M data samples which represent the statistical sample size. Thus, the process of weight optimization can be pictured as the point in time when the error sequence is orthogonal to the data sequence. The result is simply the implementation of the orthogonality principle in N -dimensions. The particular form of the LMS algorithm, introduced by Widrow and Hoff¹², makes the approximation

$$E(e_m^2) \doteq e_m^2 \quad (10)$$

thereby eliminating the need to average over a large block of data samples, which requires large storage or memory capacity. Equation (8) may now be written as,

$$W_k(m+1) = W_k(m) + 2\mu e_m x_{m-k} \quad (11)$$

which may be likened to a correlation cancellation loop (CCL)²² that removes or cancels from the output signal y_m any component of the primary input signal d_m that is correlated with the tapped data reference signal x_m . The cancellation is illustrated in figure 2 with a controlled subtraction of the tapped reference output from the primary input after the former has been adjusted in amplitude to maximize its correlation with the latter. The subtraction process continues until no correlation is detected between the output error and the reference input, at which time the mean input to the integrator is zero. Thereafter, the integrator output, which controls the amplitude adjustment, remains constant unless the input changes. The CCL has two aspects: (1) a correlation between input reference signal samples of the form: $x_{m-j}x_{m-k}$ and (2) a correlation between the primary and reference inputs of the form: $d_m x_{m-k}$.

In order to realize an N-point adaptive filter, N such CCL stages are cascaded, as illustrated in figure 2, where each CCL stage is designed to cancel a component of the primary input that is correlated with the delayed version of the reference input. The algorithm described by equation (8) and implemented in figure 2 is called the linear LMS algorithm. It requires an analog delay line with low loss and nondestructive taps to provide delayed signals (i.e., $x_1 = x(m-1)$, $x_2 = x(m-2)$, ..., $x_N = x(m-N)$)

²²D.R. Morgan, "A Note on Real-Time Linear Prediction of Speech Waveforms", IEEE Trans. Acoust. Speech, Sig. Processing., AU-21, 306 (1975).

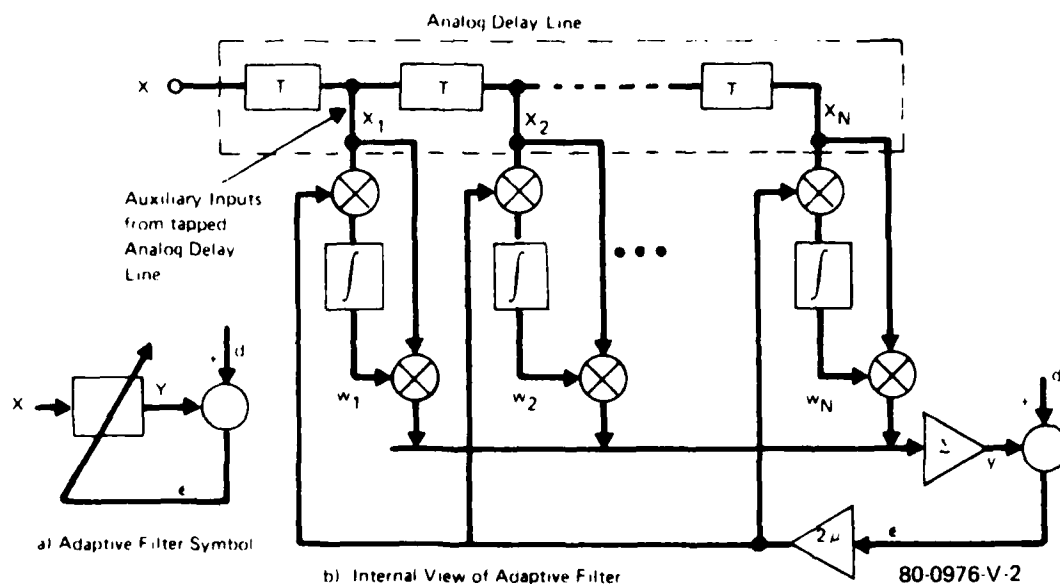


Figure 2. LMS Adaptive Filter Implemented With Linear LMS Algorithm

at the tap positions. In addition, two 4-quadrant analog multipliers and an integrator or storage element are required for each CCL stage.

The use of conventional 4-quadrant analog multipliers to implement the linear LMS algorithm is not practical. Such devices are generally expensive in discrete form, consume substantial power, and require real estate on an LSI chip. They also lack accuracy and speed which combined with the previous factors makes the 4-quadrant analog multiplier difficult to realize in integrated circuit form. Perhaps, one of the most serious drawbacks of the linear approach, is the variation in multiplier performance due to inaccuracies from such sources as dc off-sets from tap to tap. From the standpoint of usage, we note the linear LMS algorithm depends upon the reference input power level and is therefore sensitive to the variations in power level, which determines

the convergence speed of the algorithm. Thus, it is important to seek a solution to the problem of 4-quadrant analog multipliers at each tap position.

In applications where a large number of multipliers are anticipated, such as long-distance telephone communication²³, analysis has been performed²⁴⁻²⁶ that indicates the analog multipliers may be replaced by devices which can be implemented inexpensively and with characteristics quite different from the conventional multiplier. The convergence of the filter weights with nonideal multipliers²⁶ is an important property of the adaptive filter and makes such a filter very attractive for integration on a silicon chip. Thus, a form of the linear LMS algorithm, which employs a nonideal multiplier of the form

$$e_m \operatorname{sgn}(x_{m-k}) \quad (12)$$

is called the "clipped-data" LMS algorithm.²⁴ This algorithm may be written as,

$$w_k(m+1) = w_k(m) + 2\mu e_m \operatorname{sgn}(x_{m-k}) \quad (13)$$

The error, e_m , is still computed with amplitude and sign information (i.e., in a linear manner), whereas the polarity of the data reference signal is employed to determine the direction of weight adjustment. The non-linear clipper action is written mathematically as,

²³ M.M. Sondhi, "An Adaptive Echo Canceller", B.S.T.J., 46, 497 (1967).

²⁴ J.L. Moschner, "Adaptive Filter With Clipped Input Data", Stanford Lab. Rep. 6796-1, June 1970.

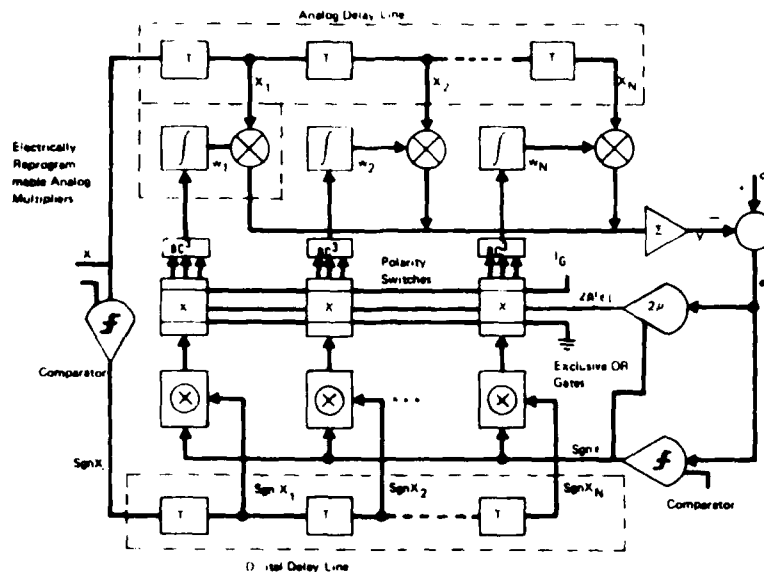
²⁵ J.R. Rosenberger and E.J. Thomas, B.S.T.J., 50, 785 (1971).

²⁶ D. Mitra and M.M. Sondhi, "Adaptive Filtering With Nonideal Multipliers--Applications to Echo Cancellation", Int. Conf. on Commun. Conf. Rec., Vol. II, 30 (1975).

$$\begin{aligned}\text{sgn}(x_{m-k}) &= +1, \text{ for } x_{m-k} \geq 0 \\ &= -1, \text{ for } x_{m-k} < 0\end{aligned}\tag{14}$$

The N linear multiplications can be replaced by N conditional branch operations which check the sign of x_{m-k} and on this basis add or subtract the quantity $2\mu e_m$ from $W_k(m)$. This elimination of N 4-quadrant multiplications provides a distinct advantage in the speed of operation for the clipped LMS algorithm without a sacrifice in the level of convergence. The speed of adaptation is reduced in comparison with the linear LMS algorithm²⁴ by a factor of $\pi/2$ for signals with Gaussian statistics.

The polarity of the reference data may be determined by a single input comparator and stored in a serial digital delay line with non-destructive parallel outputs as illustrated in figure 3. The delay line, as described later, is implemented with a CMOS shift register with parallel outputs. The analog reference input is sampled and stored in an analog delay line, implemented with a charge-coupled device (CCD) characterized by independent non-destructive read-out at the tap locations x_1, \dots, x_N . The analog and digital delay lines are synchronously clocked and each clock interval finds the analog data, x_{m-k} , and polarity data, $\text{sgn}(x_{m-k})$ available at the k^{th} tap location. The clipped-data LMS algorithm is implemented with the binary multiplication of the quantities e_m and x_{m-k} , which is accomplished by the Exclusive Or gates shown in figure 3. The output of the Exclusive Or gates controls the Polarity Switches which direct the weight update $2\mu|e_m|$ in an incremental or decremental manner. The output of the filter, y_m , is subtracted from the primary input, d_m , to form the error, e_m , and the sign is obtained with a comparator and the amplitude is obtained with a scaling, absolute-value amplifier.



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Figure 3. Clipped-Data LMS Algorithm Implementation of Adaptive Filter With Cascaded CCL's

The electrically reprogrammable analog multipliers may be multiplying digital-to-analog-converters (MDAC's)²⁷ or MOSFET's operating in their triode region, where they perform the feature of an electrically programmable analog conductance.²⁸ In the construction of the CCD Adaptive Signal Processor, the MOSFET approach is used because of its simplicity and accuracy as an analog multiplier. The disadvantages of this approach are the absence of long-term weight storage (i.e., weights must be stored on the gate capacitance of the MOSFET as accumulated charge),

²⁷Y.A. Haque and M.A. Copeland, "Design and Characterization of a Real-Time Correlator", IEEE J. of Solid-State Circuits, SC-12, 642 (1977).

²⁸M.H. White, I.A. Mack, G.M. Borsuk, D.R. Lampe, and F.J. Kub, "Charge-Coupled Device (CCD) Adaptive Discrete Analog Signal Processing", IEEE J. of Solid-State Circuits, SC-14, 132 (1979).

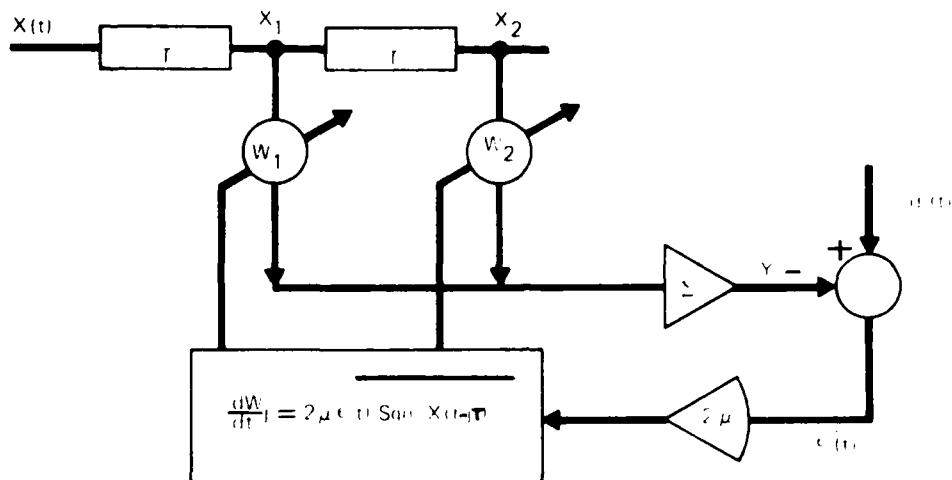
and the dc off-sets from tap-to-tap which cause non-uniformities in the multipliers. The algorithm, described in equation (13), eliminates the need for N four-quadrant analog multipliers and replaces these multipliers with conditional branching operations that are readily implemented with switches. The bidirectional charge-control circuit (BC^3) responds to the action of these switches to increment or decrement an amount of charge, which is proportional to the amplitude of the error signal, on the gate capacitance of the MOSFET analog multiplier. The integration is accomplished with the temporary storage features of the gate insulator of the MOSFET.

LMS CLIPPED DATA: ALGORITHM CHARACTERISTICS

In this section we will discuss several aspects of the LMS algorithm as applied to the "clipped-data" implementation. The two essential characteristics discussed are (1) transient response and (2) frequency selectivity. The transient response relates to the speed of convergence to achieve a desired accuracy, and the final steady-state weights of the filter. The influence of reference and desired signal amplitudes (including noise) on the transient response are particularly important in the understanding of the algorithm operation. The frequency selectivity is also of importance because the separation of narrowband and broadband signals is accomplished by the operation of the adaptive signal processor on correlated components of reference and desired signals.

(1) TRANSIENT RESPONSE OF ALGORITHM

In this section, we will present a simple analysis of a 2-tap weight adaptive filter under the control of the "clipped-data" LMS algorithm. Figure 4 illustrates a block diagram of the adaptive filter. We will analyze this adaptive filter for a sinusoidal signal in the presence of white noise. The analysis is performed for continuous signals, rather than sampled-data signals, in order to simplify the time averaging; however, the general results are applicable to sampled-data operation. A second simplification is the use of time-averaging in order to simplify



80-0976-V-4

Figure 4. A 2-Tap Weight Adaptive Filter With "Clipped Data" LMS Algorithm

the mathematics. The continuous time representation of equation (13), without the Widrow-Hoff approximation, is written as,

$$\frac{dw_j}{dt} = 2\mu \overline{e(t) x(t - jT)} \quad (15)$$

The desired signal may be written as,

$$d(t) = d_0 \cos(\omega t + \phi) \quad (16)$$

where ϕ is a relative phase-shift with respect to the signal at tap 1. The tapped reference signals are,

$$\begin{aligned} x_1(t) &= x_0 \cos(\omega t) + n_1(t) \\ x_2(t) &= x_0 \cos[\omega(t - T)] + n_2(t) \end{aligned} \quad (17)$$

where T is the time delay between tap positions and $n_1(t)$, $n_2(t)$ are uncorrelated noises at the tap positions. The matrix elements of the covariance matrix (see equation 3) become,

$$\begin{aligned}\overline{X_1(t) \operatorname{sgn}[X_1(t)]} &= \overline{(s+n_1) \operatorname{sgn}(s+n_1)} = \overline{s \operatorname{sgn} s} + \overline{n_1 \operatorname{sgn} n_1} \\ &= \frac{2X_o}{\pi} + \sqrt{\frac{2}{\pi}} \sigma_n\end{aligned}\quad (18)$$

where

$$\begin{aligned}\overline{n_1^2(t)} &= \overline{n_2^2(t)} = \sigma_n^2 \\ \overline{n_1(t)n_2(t)} &= \overline{sn_1} = \overline{sn_2} = 0\end{aligned}\quad (19)$$

Calculation of the remaining matrix elements yields

$$\begin{aligned}\overline{X_1(t) \operatorname{sgn}[X_2(t)]} &= \overline{X_2(t) \operatorname{sgn}[X_1(t)]} = \frac{2X_o}{\pi} \cos \omega T \\ \overline{d(t) \operatorname{sgn}[X_1(t)]} &= \frac{2d_o}{\pi} \cos \phi \\ \overline{d(t) \operatorname{sgn}[X_2(t)]} &= \frac{2d_o}{\pi} \cos (\omega T + \phi)\end{aligned}\quad (20)$$

which yields the weight equation (see equation 15):

$$\frac{d}{dt} \begin{pmatrix} W_1 \\ W_2 \end{pmatrix} - \frac{4\mu d_o}{\pi} \begin{pmatrix} \cos \phi \\ \cos(\omega T + \phi) \end{pmatrix} - 2\mu \begin{pmatrix} \frac{2X_o}{\pi} + \sqrt{\frac{2}{\pi}} \sigma_n & \frac{2X_o}{\pi} \cos \omega T \\ \frac{2X_o}{\pi} \cos \omega T & \frac{2X_o}{\pi} + \sqrt{\frac{2}{\pi}} \sigma_n \end{pmatrix} \begin{pmatrix} W_1 \\ W_2 \end{pmatrix} = 0 \quad (21)$$

The above equation for the weights illustrates the cross-coupling between the taps caused by the delay T and when $\omega T = (2k+1)\pi/2$, $k = 0, 1, 2, \dots$ the system is decoupled and in so-called normal form. We can transform the weights into a normal coordinate system with

$$W = \Phi \eta \quad (22)$$

where

$$\Phi = \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \quad (23)$$

is the transformation matrix. Application of this transformation to equation (21) yields

$$\frac{d}{dt} \begin{pmatrix} \eta_1 \\ \eta_2 \end{pmatrix} = \frac{4\mu d_o}{\sqrt{2} \pi} \begin{pmatrix} \cos \phi - \cos(\omega T + \phi) \\ \cos \phi + \cos(\omega T + \phi) \end{pmatrix} \quad (24)$$

$$- 2\mu \begin{pmatrix} \frac{2X_o}{\pi} (1 - \cos \omega T) + \sqrt{\frac{2}{\pi}} \sigma_n & 0 \\ 0 & \frac{2X_o}{\pi} (1 + \cos \omega T) + \sqrt{\frac{2}{\pi}} \sigma_n \end{pmatrix} \begin{pmatrix} \eta_1 \\ \eta_2 \end{pmatrix}$$

With equations (22) and (24) we can write the transient weight response of the normal weights in terms of time constants

$$\tau^- = \frac{1}{2\mu \left[\frac{2X_o}{\pi} (1 - \cos \omega T) + \sqrt{\frac{2}{\pi}} \sigma_n \right]} \quad (25)$$

$$\tau^+ = \frac{1}{2\mu \left[\frac{2X_o}{\pi} (1 + \cos \omega T) + \sqrt{\frac{2}{\pi}} \sigma_n \right]}$$

and a steady state solution for the weights becomes

$$W_1(s.s.) = \frac{d_o \left[\left(X_o + \sqrt{\frac{\pi}{2}} \sigma_n \right) \cos \phi - X_o \cos \omega T \cos(\omega T + \phi) \right]}{\left(X_o + \sqrt{\frac{\pi}{2}} \sigma_n \right)^2 + \cos^2 \omega T} \quad (26)$$

$$W_2(s.s.) = \frac{d_o \left[\left(X_o + \sqrt{\frac{\pi}{2}} \sigma_n \right) \cos(\omega T + \phi) - X_o \cos \phi \cos \omega T \right]}{\left(X_o + \sqrt{\frac{\pi}{2}} \sigma_n \right)^2 + \cos^2 \omega T}$$

which we observe is a function of frequency providing $\omega T \neq (2k + 1)\pi/2$, $k = 0, 1, 2, \dots$. When this condition is approached, the optimal weights approach the values,

$$W_1 (\text{opt.}) \rightarrow \frac{d_o \cos \phi}{X_o + \sqrt{\frac{\pi}{2}} \sigma_n} \quad (27)$$

$$W_2 (\text{opt.}) \rightarrow \frac{-d_o \sin \phi}{X_o + \sqrt{\frac{\pi}{2}} \sigma_n} \quad \omega T \simeq (2k + 1) \pi/2$$

and the weights are decoupled from one another as the coordinate system approaches normal form.

Glover²⁹ has analyzed the particular case when there is a 90-degree phase shift between the weights for adaptive noise cancelling in the form of a notch filter. He showed when a sum of sinusoids is applied to an adaptive filter, the filter converges to a dynamic solution in which the weights are time varying. This time-varying solution gives rise to a tunable notch filter with a notch located at each of the reference frequencies. In the example considered, the desired and reference inputs were operating at the same frequency (i.e., $f_d = f_r$). Glover showed²⁹ for $f_d \neq f_r$ the weights have a dynamic steady-state response with an oscillation at the difference frequency $f_d - f_r$ and the instantaneous response at f_r . This time-varying solution should not be considered as noise in the adaptation process. In essence, the time-varying weights modulate the reference frequency f_r and heterodyne it into the desired frequency f_d , thus, creating a notch effect.

²⁹J.R. Glover, "Adaptive Noise Cancelling of Sinusoidal Interference", Naval Underseas Center, San Diego, Calif. Rept # TN 1617, Dec. 1975. (Stanford University Ph.D. Thesis).

(2) A 2-TAP ADAPTIVE FILTER

In this section we will examine a simple single-frequency noise canceller with 2-adaptive weights under the operation of the "clipped data" LMS algorithm. Figure 5 illustrates the single frequency noise canceller in which the desired input may be any type of signal (i.e., stochastic, deterministic, periodic, transient, or combination thereof) while the input signal is a pure cosine wave $X_0 \cos(\omega_0 t - \phi)$. The desired and input signals are sampled synchronously at $f_c = 1/T$ with a 90 degree phase between X_1 and X_2 taps. The algorithm for updating the weights is,

$$\begin{aligned} W_1(m+1) &= W_1(m) + 2\mu \epsilon(m) \operatorname{sgn}[X_1(m)] \\ W_2(m+1) &= W_2(m) + 2\mu \epsilon(m) \operatorname{sgn}[X_2(m)] \end{aligned} \quad (28)$$

where,

$$\begin{aligned} X_1(m) &= X_0 \cos(\omega_0 mT - \phi) \\ X_2(m) &= X_0 \sin(\omega_0 mT - \phi) \end{aligned} \quad (29)$$

The first step in the analysis is to consider the adaptive noise canceller as a feedback network with the filter output $Y(m)$ disconnected. Under these conditions, a unit impulse at $m = k$ is applied at the desired input to create an error,

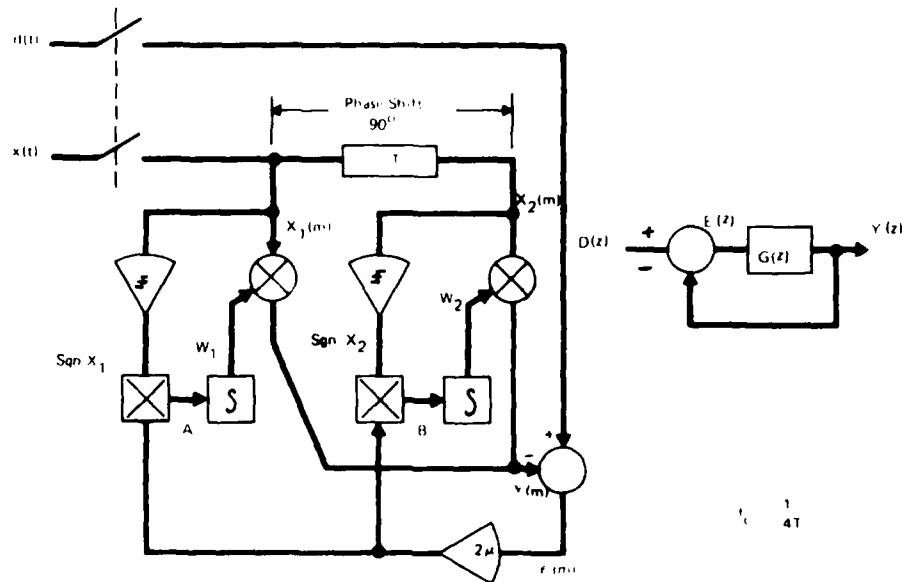
$$\epsilon(m) = \delta(m-k) \begin{cases} 1 & m=k \\ 0 & m \neq k \end{cases} \quad (30)$$

The transfer function of the incremental weight change may be written as,

$$z \{ W_1(m+1) - W_1(m) \} = (Z-1) W_1(Z) \quad (31)$$

or

$$W_1(Z) = U(Z) z \{ 2\mu \epsilon(m) \operatorname{sgn}[X_1(m)] \} \quad (32)$$



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Figure 5. Single Frequency Adaptive Noise Canceller

where $U(Z) = (Z-1)^{-1}$. The impulse response of $U(Z)$ is the step response,

$$u(m-1) = \begin{cases} 1 & m \geq 1 \\ 0 & m < 1 \end{cases} \quad (33)$$

Convolution of $u(m-1)$ with $2\mu \epsilon(m) \text{sgn} [X_1(m)]$ yields the weight,

$$W_1(m) = 2\mu \text{sgn} [\cos(\omega_0 kT - \phi)] \quad m \geq k+1 \quad (34)$$

and the corresponding filter output is,

$$Y_1(m) = 2\mu X_0 \cos(\omega_0 mT - \phi) \text{sgn} [\cos(\omega_0 kT - \phi)] \quad m \geq k+1 \quad (35)$$

Similarly,

$$Y_2(m) = 2\mu X_0 \sin(\omega_0 mT - \phi) \text{sgn} [\sin(\omega_0 kT - \phi)] \quad m \geq k+1 \quad (36)$$

with the total output,

$$Y(m) = Y_1(m) + Y_2(m) = 2\mu X_o \left[\cos(\omega_o mT - \phi) \operatorname{sgn} [\cos(\omega_o kT - \phi)] \right. \\ \left. + \sin(\omega_o mT - \phi) \operatorname{sgn} [\sin(\omega_o kT - \phi)] \right] \quad m \geq k+1 \quad (37)$$

Equations 30 and 37 may be Z-transformed to yield the pulse transfer function.

$$G(Z, k) = 2\mu \sqrt{2} X_o \frac{\left\{ Z \cos [(k+1)\omega_o T - \phi - \pi/4] - \cos [k\omega_o T - \phi - \pi/4] \right\}}{Z^2 - 2Z \cos \omega_o T + 1} \quad (38)$$

where $0^\circ \leq k\omega_o T - \phi \leq \pi/2$, since the above transfer function repeats every 90 degrees. In the above form, $G(Z, k)$ is nontime-invariant, and in order to remove the k -dependence, we will average over the period indicated to obtain

$$\overline{G(Z)} = \frac{8\mu X_o}{\pi} \frac{(Z \cos \omega_o T - 1)}{Z^2 - 2Z \cos \omega_o T + 1} \quad (39)$$

Since the closed-loop transfer function is

$$H(Z) = \frac{E(Z)}{D(Z)} = \frac{1}{1 + \overline{G(Z)}} \quad (40)$$

with closed-loop zeroes given as

$$Z = e^{\pm j\omega_o T} \quad (41)$$

and poles from the solution of $1 + \overline{G(Z)} = 0$. If we make the narrowband approximation with $\mu X_o < 1$, then the poles are inside the unit circle with a radial distance.

$$\left(1 - 8\mu \frac{X_o}{\pi} \right)^{1/2} \approx 1 - 4\mu \frac{X_o}{\pi} \quad (42)$$

from the origin as shown in figure 6. The angles of the poles are almost identical to those of the zeroes with a notch filter bandwidth

$$B.W. = \frac{8\mu X_o}{\pi T} \quad (43)$$

with a Q,

$$Q = \frac{\omega_o}{B.W.} = \frac{\pi}{8} \frac{\omega_o T}{\mu X_o} \quad (44)$$

A special case of the notch filter is to set $\omega_o = 0$ in equations 39 and 40 to yield

$$H(Z, \omega_o = 0) = \frac{Z - 1}{Z - (1 - 8 \frac{\mu X_o}{\pi})} \quad (45)$$

which places the notch at zero frequency to cancel low frequency drift. Since there is no need to match the phase of the signal, only one weight is needed. The bandwidth is given by equation 43 and the transfer function, expressed by equation 45, indicates a pole-zero separation of,

$$\frac{8\mu X_o}{\pi}$$

on the real axis. The use of a bias weight can remove slowly varying drift components in the input signal and may be used simultaneously with operation to cancel periodic or stochastic interference.

III. CCD MONOLITHIC ADAPTIVE SIGNAL PROCESSOR

ADAPTIVE FILTER GENERALIZED BLOCK DIAGRAM

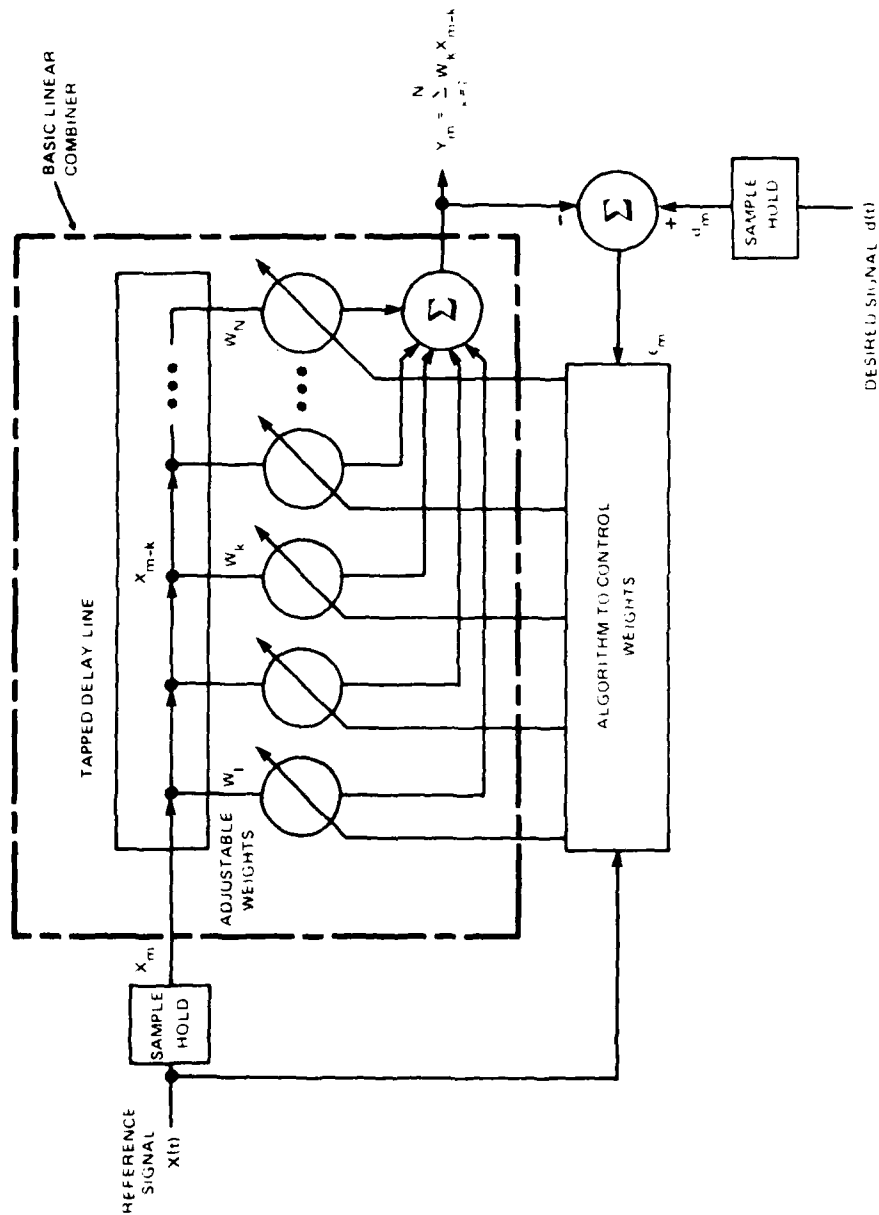
Illustrated in figure 7 is a generalized block diagram of an adaptive filter for a sampled data system. The input reference signal, $x(t)$, and desired signal, $d(t)$, are continuous time signals which are converted to sampled data system format via the sample and hold circuit at each input. The signals, which are selected for the reference and desired inputs, will be determined by the adaptive filter application. Section V describes these application areas.

The samples of the reference signal, x_m , are applied to an N-stage, tapped, delay line. The output of each tap, x_{m-k} , is multiplied by an adjustable weight, W_k , and an output signal, y_m , is formed via the simultaneous summation of the weighted products, to yield

$$y_m = \sum_{k=1}^N W_k x_{m-k} \quad (1)$$

which is the discrete convolution of the tap weights and tapped delay line outputs. The transversal filter output is subtracted from the desired signal to form an error signal, e_m , which is applied, together with the reference signal, x_m , to an algorithm which adjusts all weights simultaneously at each clock iteration until the mean-squared-error (MSE) is minimized. The weight control algorithm used on this monolithic adaptive filter chip is the "clipped-data" LMS algorithm¹ and requires that the weight at the k^{th} tap location during the m^{th} clock period be updated

¹J.L. Moschner, "Adaptive Filter with Clipped Input Data", Stanford Lab. Rep. 6796-1, June 1970.



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Figure 7. Adaptive Filter Block Diagram

according to the equation,

$$W_k(m+1) = W_k(m) + 2\mu e_m \operatorname{sgn}(x_{m-k}) \quad (2)$$

where,

$$e_m = d_m - y_m \quad (3)$$

which is explained in Section II.

In order to see the development of the monolithic chip, we may rewrite equation (2) as

$$W_k(m+1) = W_k(0) + 2\mu \sum_{j=1}^m \operatorname{sgn}(x_{j-k}) \operatorname{sgn}(e_j) |e_j| \quad (4)$$

over m data samples, which represents the statistical sample size (e.g., see equation (9) in Section II). Equation (4) describes the basic requirements to implement the adaptive filter, namely,

1. At each clock period, j , the sign of the error, e , and the sign of the reference data at each tap position, x_{j-k} , must be determined.
2. At each clock period, j , the weight at each tap location, $W_k(m)$, must be incremented with

$$\operatorname{sgn}(x_{j-k}) \operatorname{sgn}(e_j) > 0$$

or decremented with

$$\operatorname{sgn}(x_{m-k}) \operatorname{sgn}(e_j) < 0$$

by an amount $2\mu \cdot |e_j|$, where " μ " is the convergence factor.

3. The weight value at each tap location must be the integrated sum of all previous weight increments and decrements. A storage element is therefore required at each tap location.

A detailed block diagram of the monolithic adaptive filter chip, incorporating the above requirements is shown in figure 8. Operation of the circuit will be described with reference to the features shown in the figure.

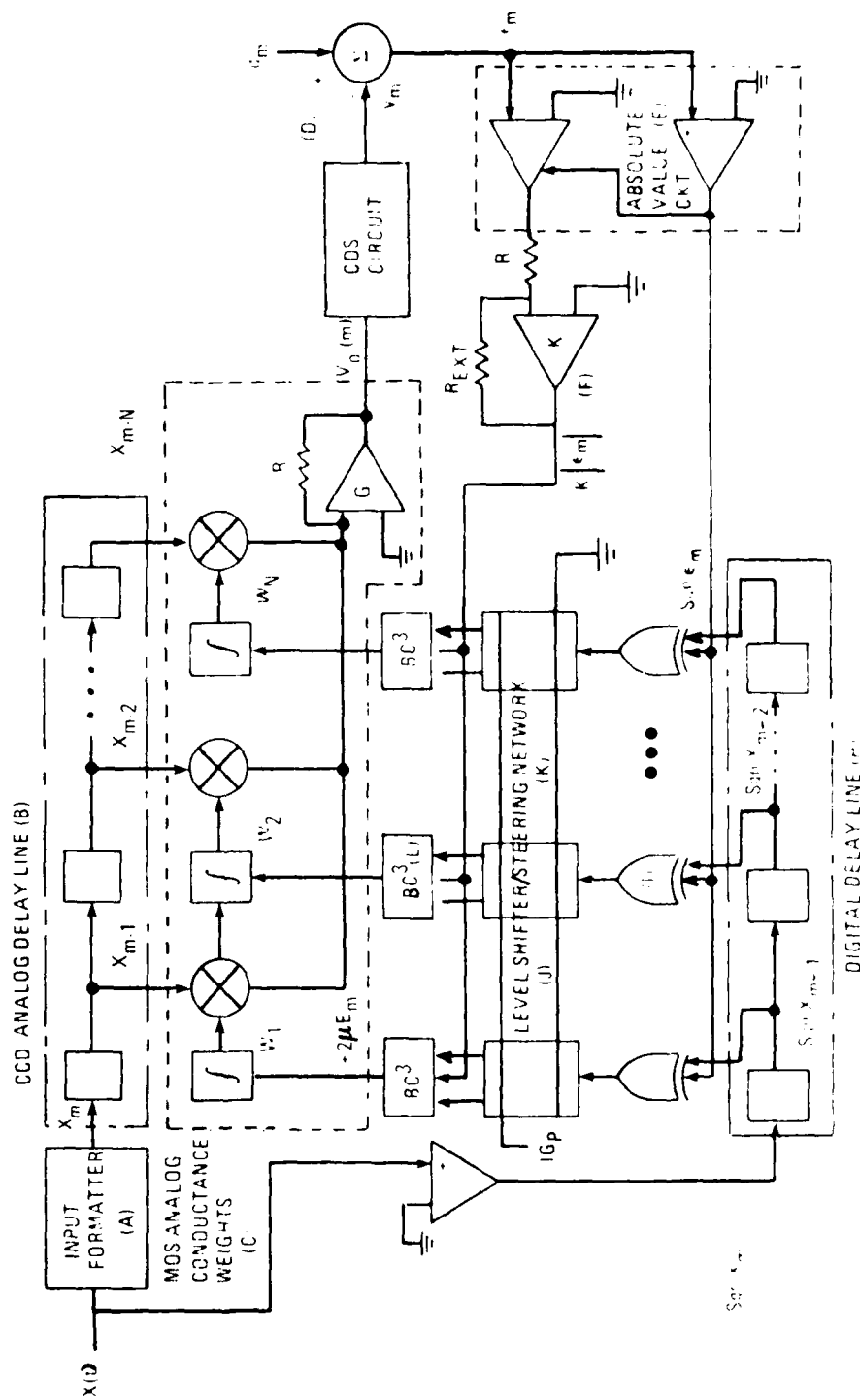


Figure 8. Detailed Block Diagram of Monolithic Adaptive Filter

(1) The analog signal, $x(t)$, is converted to a sampled data format, which is compatible with the architecture of the analog delay line, by the input formatter circuit.

(2) The formatter output voltage, x_m , is applied to the input of a p-channel CCD analog delay line, operating in the so-called "surface-channel" mode. The input voltage is converted to charge with a stabilized charge injection circuit² and the resulting charge packet is transferred along the length of the CCD (Charge-Coupled Device) by a 2-1/2 phase clocking sequence.³

(3) At each tap location, the charge packet is nondestructively sensed and converted back to a voltage by a floating clock electrode sensor circuit.⁴

(4) Each tap output voltage is multiplied by a programmable analog conductance multiplier which converts the output voltage to a weighted current. An analog signal processor simultaneously sums all currents, performs current to voltage conversion with a transconductance amplifier, and a clamp/sample operation produces the transversal filter output, y_m . The error is formed by subtracting y_m from d_m , a sampled version of the desired input signal.

(5) The algorithm requires three operations to be performed on the error:

(a) Form the absolute value of the error, $|e_m|$

²M.H. White, D.R. Lampe, F.C. Blaha, and I.A. Mack, "CCD and MNOS Devices for Programmable Analog Signal Processing and Digital Nonvolatile Memory", 1973 IEEE Int'l Electron Devices Meeting (IEDM), Washington, D.C.

³M.H. White, I.A. Mack, G.M. Borsuk, D.R. Lampe, and F.J. Kub, "CCD Analog Adaptive Signal Processing", 1978 Int'l Conference on the Applications of CCD's, San Diego, Calif.

⁴M.H. White, I.A. Mack, F.J. Kub, D.R. Lampe, and J.L. Fagan, "An Analog CCD Transversal Filter with Floating Clock Sensor and Variable Tap Gains", 1976 IEEE Int'l Solid-State Circuits Conf., (ISSCC), Philadelphia, Pa.

(b) Scale the error by 2μ

(c) Form the sign of the error, $\text{sgn}(e_m)$

The sign of the error is formed by a comparator and is subsequently used in an absolute-value circuit. The absolute value circuit output is scaled by a factor "K", where "K" contributes to the overall convergence factor, 2μ .

(6) To eliminate the requirement of a comparator at each tap location to form $\text{sgn}(x_{m-k})$, a single comparator is employed at the adaptive filter input to form the sign of each reference input signal. The comparator output, $\text{sgn}(x_m)$, is inputted to a digital shift register, which is clocked in unison with the corresponding analog samples in the CCD.

(7) The $\text{sgn}(x_{m-k}) \text{sgn}(e_m)$ product is formed in an Exclusive OR circuit, with one Exclusive OR circuit for each CCD tap required. The Exclusive OR circuit provides a binary multiply of the delayed sign of the reference input signal and the sign of the error, with N such multiplies accomplished, in parallel, for each clock period. The output of the Exclusive OR circuit, at each tap location, determines whether or not the particular weight in question will be incremented or decremented. A steering network, at each tap location, programs the electrode configuration of a Bidirectional Charge Control Circuit (BC^3) to either increment or decrement the weight by adjusting the polarity of the quantity, $2\mu |e_m|$.

DESCRIPTION OF BASIC COMPONENTS

The following sections will illustrate the operation of the basic components which are incorporated on the monolithic chip of the CCD Adaptive Signal Processor.

A. INPUT FORMATTER CIRCUIT

The input formatter circuit converts the continuous time reference input signal, $x(t)$, into a sampled data signal with a format compatible with the organization of the CCD tapped delay line

and the format requirements of the correlated double sampling⁵ (CDS) circuit which is located in the clamp/sample operation of the analog signal processor. With reference to figure 9a the circuit operation is as follows:

(1) "AC Zero" Clamp Operation

With ϕ_I high Q_2 and Q_3 are conducting while Q_1 is off, allowing C (≈ 10 pF) to charge to the ac zero or CCD so-called "fat-zero" voltage, V_{FZ} .

(2) Signal Sample Operation

With ϕ_I low, Q_1 conducts while Q_2 and Q_3 are off. With no input sample, this permits C to "float" and to act as a battery with a voltage V_{FZ} relative to the input, providing the "off" resistance of the switches and the capacitance have a time constant which is long compared with the input sampling frequency. With a signal $x(t)$ applied to the input, the input to the amplifier becomes the signal voltage $x(t)$ superimposed upon the voltage across the capacitor C. If the input signal is "riding" on a dc level, X_{dc} , the amplifier output voltage, in the absence of amplifier offsets and clock feedthroughs, which are reduced with the use of "dummy" transistors Q_4 , Q_5 and Q_6 , is given by

$$\text{"signal + AC zero": } X'_m = x_m + X_{dc} + V_{FZ} \quad (5)$$

$$\text{"AC zero": } X'_m = V_{FZ}$$

where X'_m consists of two parts during the m^{th} clock period. Figure 9b shows a photomicrograph of the input formatter and figure 10 illustrates the continuous time input and the resulting "signal + AC zero" and "AC zero" formatted output.

⁵M.H. White, D.R. Lampe, I.A. Mack, and F.C. Blaha, "Characterization of Surface Channel CCD Image Arrays at Low Light Levels", IEEE J. of Solid-State Circuits, SC-9, 1 (1974).

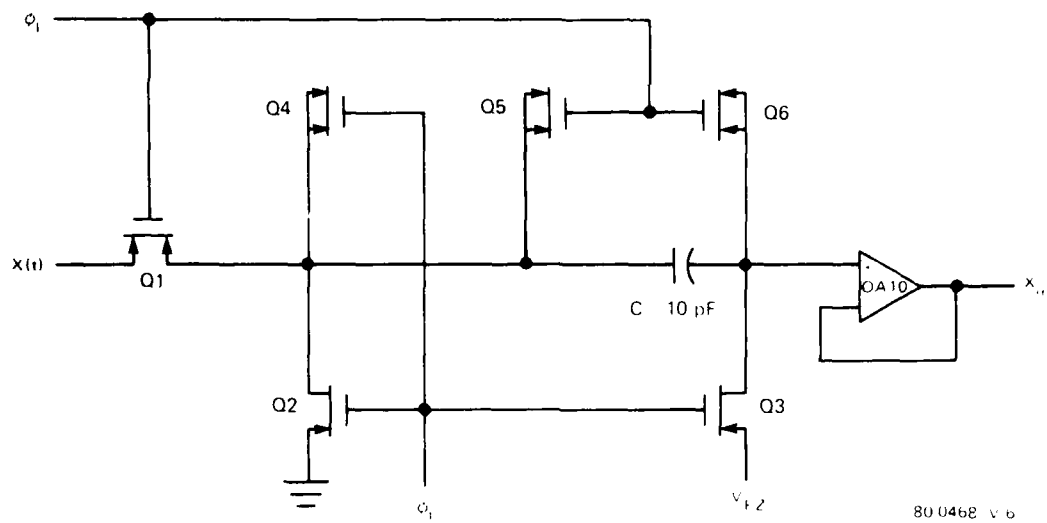


Figure 9a. Input Formatter Circuit

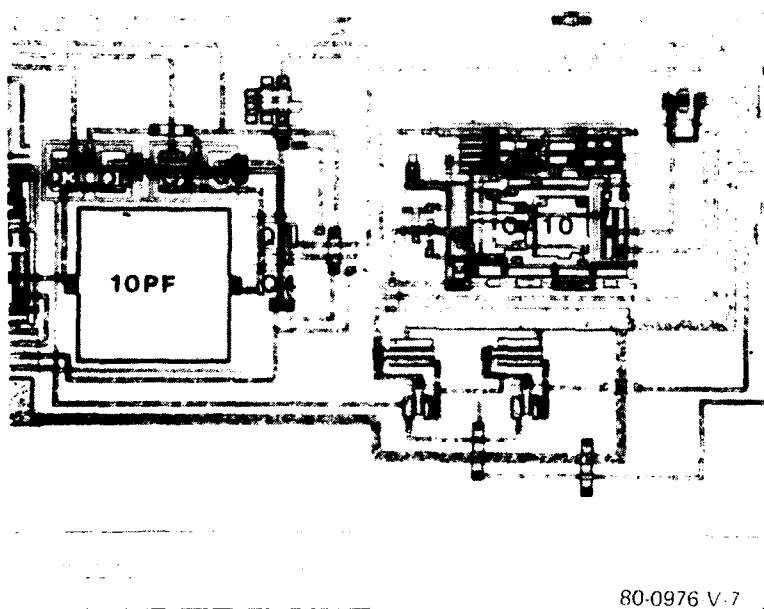


Figure 9b. Photomicrograph of Input Formatter Circuit

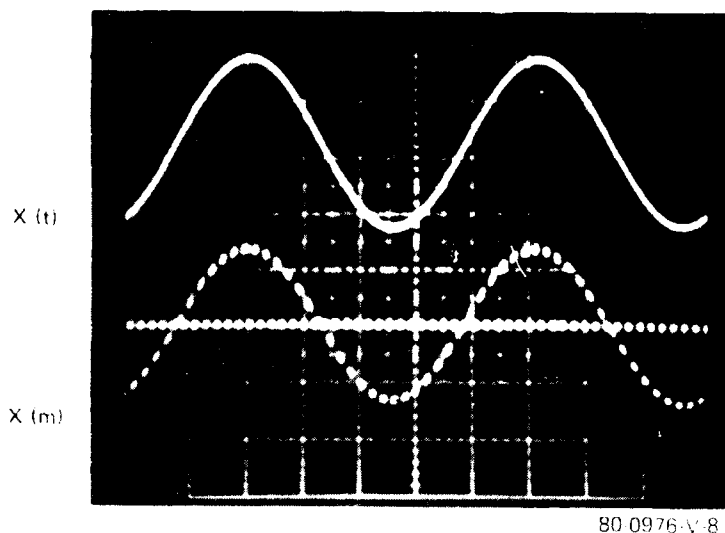


Figure 10. Input Formatter Circuit Operation

B. TAPPED ANALOG DELAY LINE

The CCD, which is used as a tapped analog delay line, is a p-type, Surface Channel, structure and is shown in figure 11 along with the associated timing diagram. The input signal, x_m , is converted to a charge and injected into the CCD with a stabilized charge injection circuit to provide low noise, linear operation.² Subsequently, the charge is clocked along the CCD in the manner described in figure 11a. The clocking scheme and electrode configuration is designed to minimize the complexity of the circuitry needed to generate the CCD clocks and also to minimize ϕ_2 clock feed-throughs to the sensing node of the floating clock electrode sensor circuit. These feed-throughs are minimized by inserting a "shield" between the ϕ_2 clock electrode and the sensing electrode. The "shield" is provided by the dc voltage, V_{FG} , on one side of the sensing node, and by the low "on" resistance of the ϕ_1 clock driver on the other side of the sensing node. We examine the

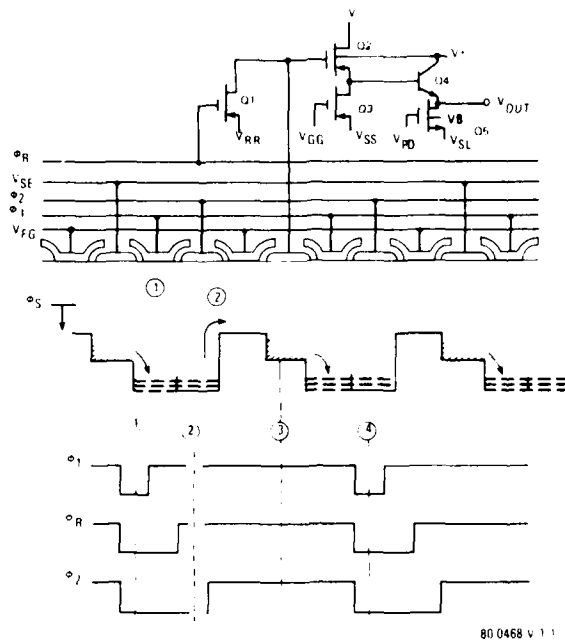


Figure 11a. 2-1/2 ϕ CCD With NDRO

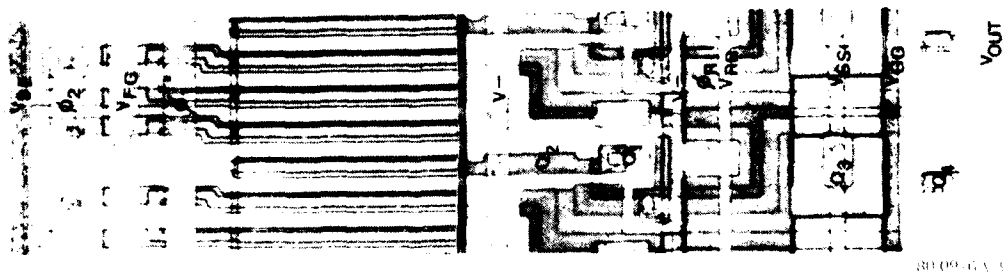


Figure 11b. Photomicrograph of CCD and NDRO Circuit

operation of the nondestructive sensing circuit with reference to figure 11a. At time ①, a charge packet is in "wells" under electrodes clocked by ϕ_1 and ϕ_2 , while the sensing electrode is reset to V_{RR} by the reset switch, enabled by ϕ_R . At time ②, ϕ_1 , ϕ_2 and ϕ_R have been pulsed to a voltage near substrate potential, forcing charge over the potential barriers controlled by a dc voltage, V_{FG} , and under the sensing electrode of the floating clock electrode sensing (FCES) circuit. The charge packet causes a change in surface potential, which is sensed on the gate of MOS FET Q_2 . At time ③, after stabilization of the voltage on the sensing electrode, a clamp (sample) operation is performed in the CDS circuit. At time ④, the cycle is repeated by enabling ϕ_1 , ϕ_R , and ϕ_2 .

The FCES circuit is composed of the reset switch, Q_1 sensing amplifier, Q_2 , source-follower load amplifier, Q_3 , and an emitter-follower, bipolar transistor, Q_4 for a low-output impedance buffer. The source-follower configuration minimizes tap-to-tap gain variations⁶ in contrast with inverting-type configurations. The N-channel MOSFET with gate-control voltage, V_{PD} , is connected in parallel with the tap-weight (not shown) in order to "sink" the dc bias current of the bipolar transistor. This minimizes the voltage drop across the analog conductance MOSFET tap weight and the current-sinking requirements of the summing transconductance amplifier.

The 2-1/2 ϕ CCD clock technique provides a simplified timing sequence and reduces clock feedthroughs as compared with a 4- ϕ clock sequence⁶; however, there is a reduction in charge-handling capability and transfer efficiency which is not a restriction in the present design. The maximum desired output from each tap is approximately 0.2 V peak-to-peak to maintain the MOSFET analog

⁶Final Report, "CCD Adaptive Discrete Analog Signal Processing", Contract No. N00173-76-C-0147, July 1977.

conductance multiplier in a linear region of operation⁷ and a large charge-handling capability is not essential. The maximum frequency of sampled operation is approximately 100 KHz and transfer efficiency above these frequencies is not required in the processor. This limit is imposed by the bandwidth of the analog operational amplifiers which determines the time required to reach at 1 percent accuracy (settling time) in the clamp/sample operation of the analog signal processor. A photomicrograph of a non-destructive readout circuit (NDRO) for CCD signal charge is shown in figure 11b, while the impulse response at the 1st, 8th, and 16th taps is illustrated in figure 12.

C. MOS PROGRAMMABLE ANALOG CONDUCTANCE WEIGHT

The circuit used to implement a programmable analog conductance weight is illustrated in figure 13. The variable weighting function is performed by a MOS Transistor biased in the triode region⁸ with an initial multiplication determined by the analog conductance,

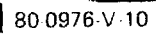
$$g_{DS} = \bar{\mu} C_O (W/L) (V_{GS} - V_T) \quad (6)$$

where $\bar{\mu}$ is the effective carrier (electron) mobility, C_O the effective oxide capacitance/area, W/L the width-to-length ratio, V_{GS} the effective gate-to-source voltage, and

$$V_T = V_{TO} + \lambda [(V_{BS} + \phi)^{1/2} - \phi^{1/2}] \quad (7)$$

⁷D.R. Lampe, H.C. Lin, M.H. White, I.A. Mack, "Fourier Analysis Computer Aided Design (CAD) of CCD Signal Processing Analog Multipliers Arrays", 1976 Conference on CCD Technology and Applications, Washington, D.C.

⁸M.H. White, I.A. Mack, G.M. Borsuk, D.R. Lampe, and F.J. Kub, "Charge-Coupled Device (CCD) Adaptive Discrete Analog Signal Processing", IEEE J. of Solid-State Circuits, SC-14, 132 (1979).



80 0468 V 14 1

Figure 13. Weight Circuit

where V_{TO} is the zero-bias ($V_{BS} = 0$) threshold voltage, ϕ the surface potential in strong inversion $\phi = 2\phi_F$, V_{BS} the bulk to source bias, and $\lambda = (2K_S \epsilon_0 q N)^{1/2} / C_O$, the so-called "body-factor". The tapped delay line output voltage is multiplied by g_{DS} , the drain-to-source analog conductance of the N-channel MOSFET, and the resulting current is converted to a voltage by operational amplifiers OA1 or OA2, depending upon the signal path from the tapped output voltage. In order to realize a positive or negative effective weight, two MOSFET's must be used at each tap location. The gate voltage, V_{GW}^- of one MOSFET is adjusted so its fixed conductance bisects the dynamic range of the programmable conductance with designated gate Voltage, V_{GW}^+ . This latter conductance represents the programmable weight which is connected to the BC^3 circuit. Thus, the function of V_{GW}^+ is to vary above or below the value of V_{GW}^- in order to determine an effective positive or negative weighted voltage at the output, $v_o(m)$. The effective weight is given by the expression,

$$W_k(m) = v_o(m) / x_{m-k} = \frac{R_5}{R_3} R_1 \bar{\mu} C_O (W/L) [V_{GW}^+(m) - V_{GW}^-] \quad (7)$$

if the individual resistors, W/L 's, etc... are matched.

The gate voltage of the variable analog conductances can be controlled by the output of the BC^3 circuit or programmed externally with W_{ext} by the action of $P\phi_{G3}$ and dc enable gate signal, V_{WR} , on the external program enable transistor. With the 16 taps on the CCD at their maximum differential conductance (i.e., approximately 15 $K\Omega$ per tap weight), and a 0.2 V peak-to-peak excursion at each tap location, the maximum value of $v_o(m)$ is approximately 4.3 V when all resistors equal 20 $K\Omega$, which is within the common-mode range of the CMOS Operational Amplifiers operating at ± 7.5 V supply voltages.

D. CORRELATED DOUBLE SAMPLING (CDS) AND DIFFERENCE CIRCUIT

In reference to figure 14 the circuitry enclosed within the dotted lines is the CDS circuit⁵ which is employed to difference the "ac zero" and "Signal + ac zero" formatted signal appearing at the output of the "weighting" circuit. For implementation on a monolithic chip, the CDS circuit could have been realized by connecting the clamp capacitor, C_c , directly to the sampling switch (controlled by ϕ_s) in order to eliminate the amplifier OA4. This approach has two major drawbacks, namely, (1) the sampled signal is attenuated by capacitive voltage division between the clamp and sample capacitors (i.e., by the ratio $C_c/(C_c+C_s)$), and (2) a "dump" switch to ground across C_s is required to initialize the sample capacitor prior to each new sample acquisition. This would result in additional timing waveform complexity and an additional "level" in the output waveform. The use of the buffer amplifier, although consuming more power, provides a voltage source driver for the sample capacitor, which eliminates the need for a dump switch and provides a continuous output signal over the sample interval.

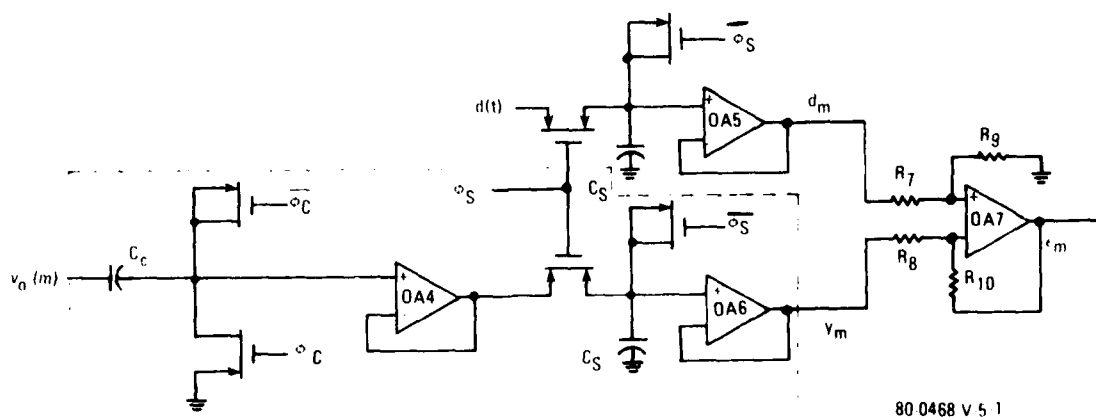


Figure 14. CDS and Difference Circuit

The output signal, y_m , is the transversal filter output. During the y-channel sampling interval, the desired signal, $d(t)$, is also sampled. This action, although band-limiting the d-channel, provides a complementary, stationary, signal to the difference amplifier. The error, $e_m = d_m - y_m$, is formed by the difference amplifier OA7 with resistor values of $R_7, R_8 = 10 \text{ K}\Omega$, $R_9, R_{10} = 20 \text{ K}\Omega$. Operational amplifiers OA4, OA5, and OA6 function as unity-gain buffer amplifiers in the voltage-follower mode.

E. ABSOLUTE VALUE CIRCUIT

The absolute value circuit, shown in figure 15a, uses $\text{sgn}(e_m)$ to control the transfer function of an operational amplifier, OA8. The sign of the error, e_m , is determined by an operational amplifier, C_e , which is operated in the open-loop, high-gain, mode as a comparator. In this mode the internal compensating capacitor is removed in order to ensure maximum gain at a specified clocking rate. The output of C_e is translated to a low-level, logic signal (0 to +7.5 V) with a CMOS inverter pair to

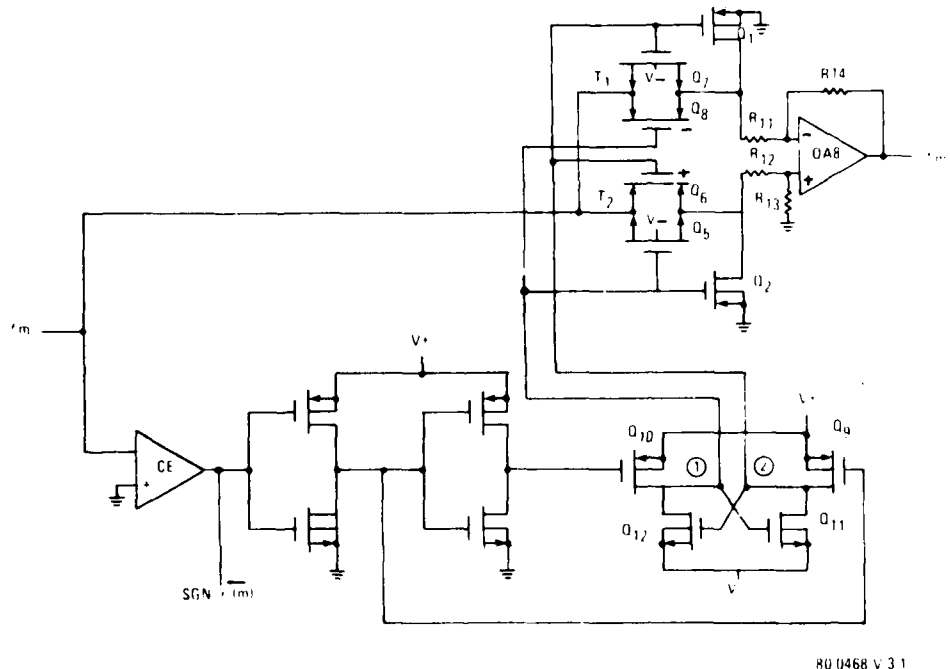


Figure 15a. Absolute Value Circuit

provide complementary drive signals to a ± 7.5 V level shifter which in-turn provides the necessary drive signals to the CMOS transfer gates, T1 and T2. When the error signal $e_m > 0$, node 1 of the level shifter is negative while node 2 is positive. Thus, T1 and Q₂ are OFF, while T2 and Q₁ are conducting or "ON". This places the amplifier in a non-inverting configuration with the transfer function,

$$\frac{|e_m|}{e_m} = \frac{R_{13}}{R_{ON}(T2) + R_{12} + R_{13}} \left[1 + \frac{R_{14}}{R_{ON}(Q_1) + R_{11}} \right] \underline{\underline{e_m > 0}} \quad (8)$$

With the input signal $e_m < 0$, T1 and Q2 are conducting, ON, while Q1 and T2 are OFF. This places the amplifier OA8 in an inverting configuration with the transfer function,

$$\frac{|e_m|}{e_m} = \frac{R_{14}}{R_{ON}(T1) + R_{11}} \underline{\underline{e_m < 0}} \quad (9)$$

The resistors of the operational amplifier, designed for $20 \text{ K}\Omega$, are much larger than the ON resistance of the MOS transistors when driven with the 15 V range of the level shifters. Thus, there is very little gain difference between the inverting and non-inverting configurations. A photomicrograph of the absolute value circuit is shown in figure 15b and the circuit operation is illustrated in figure 16.

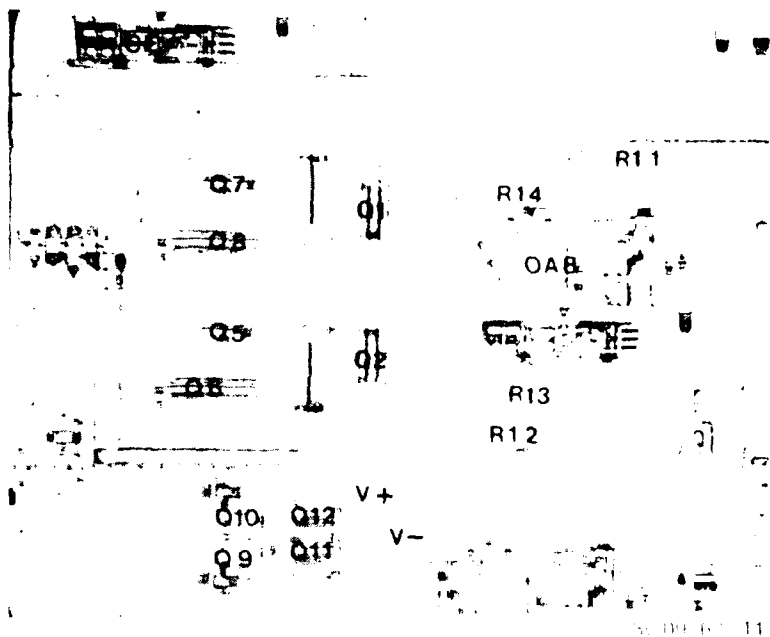


Figure 15b. Photomicrograph of Absolute Value Circuit

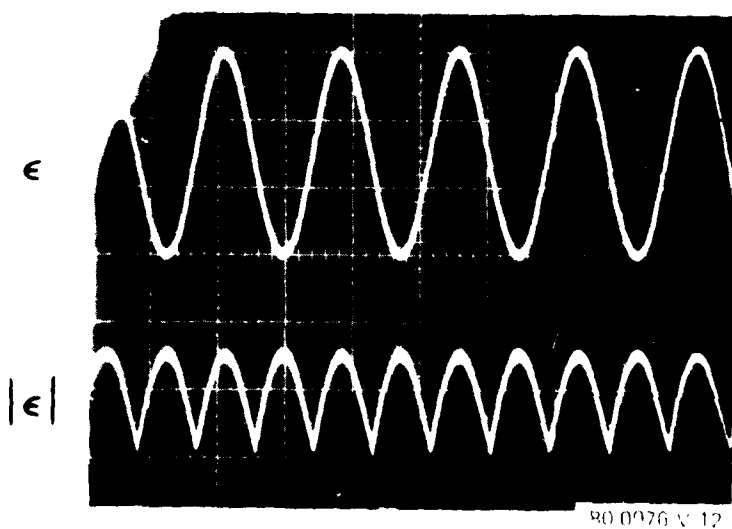


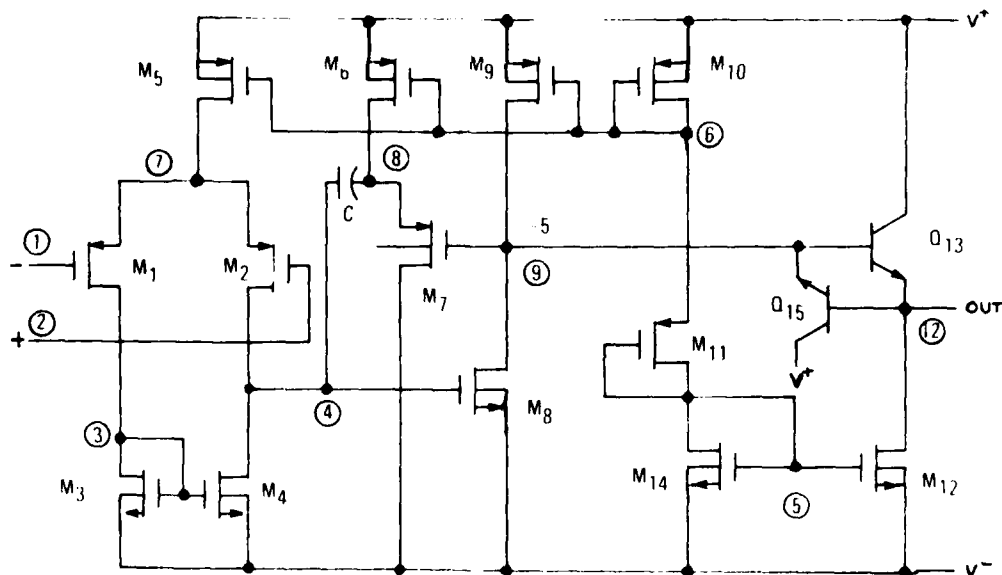
Figure 16. Absolute Value Circuit Operation

F. SCALING AMPLIFIER

The output of the absolute value circuit is applied to an inverting amplifier with an off-chip resistor to allow external selection of the convergence factor, μ . The output of the scaling amplifier is the analog signal which determines the magnitude of the weight change at each tap location.

G. OPERATIONAL AMPLIFIERS

The operational amplifier is a primary component of the CCD adaptive signal processor because it is utilized in many different operations. One amplifier design is used as the basis for a comparator, buffer or voltage-follower amplifier, difference amplifier, absolute-value amplifier, scaling amplifier, and current-to-voltage converter. Twelve amplifiers are used to realize these various functions. The amplifier design⁸, shown in figure 17a with a photomicrograph shown in figure 17b, is based upon design



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Figure 17a. CMOS Operational Amplifier Schematic

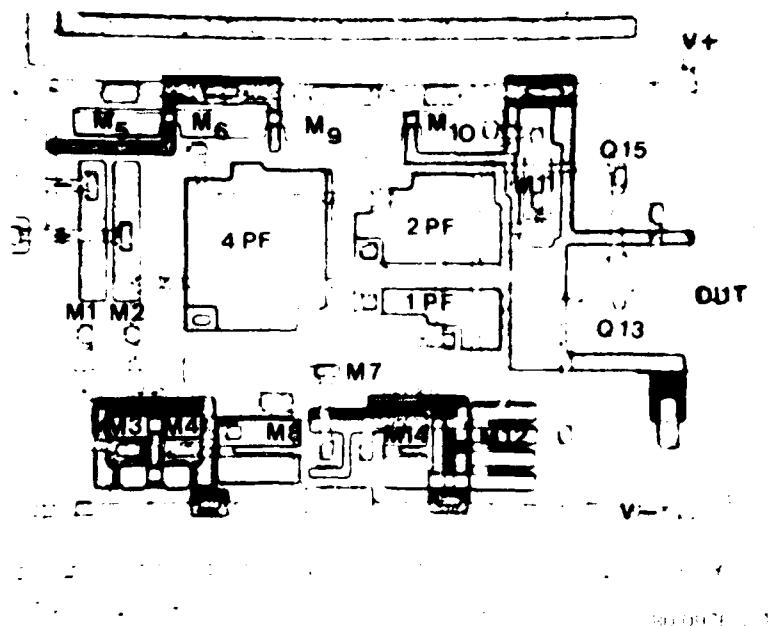


Figure 17b. Photomicrograph of CMOS Operational Amplifier
(12 Mils x 15 Mils)

practices employed in bipolar amplifiers⁹, where NPN bipolar transistors become NMOS transistors and lateral PNP bipolar transistors become PMOS transistors. Thus, CMOS design¹⁰ is quite analogous to bipolar design with internal frequency compensation provided by the capacitance C in a special, source-follower, buffered 2nd stage.¹¹

⁹J.E. Solomon, "The Monolithic Op Amp: A Tutorial Study", IEEE J. of Solid State Circuits, SC-9, 314 (1974).

¹⁰G.F. Landsburg, "A Two-Chip CMOS CODEC", IEEE Solid-State Circuits Conference, 1978, p. 180.

¹¹Y.P. Tsividis and P.R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation", IEEE J. Solid-State Circuits, SC-11, 748 (1976)

The CMOS amplifier has an input differential stage with PMOS input transistors to provide low off-set voltages and low 1/f noise. The differential input to single-ended output is accomplished with active loading formed by NMOS transistor M4. The output of the differential stage is applied to a high-gain CMOS level-shifter/gain stage formed by the inverter M8-M9 whose output, at node 9, is fed back to the inverter input (node 4) by means of a unity gain buffer (source-follower) stage formed by M6 and M7. The source-follower buffers the compensation capacitor C to reduce the phase shift associated with the forward transmission in the gain-stage M8-M9. The emitter-follower output stage provides a low output impedance for driving with a fast positive slewing rate. M12 must be selected so as to sink the discharge current from the load capacitance, which sets the limit on the negative slewing rate. The input stage differential drain currents determine the internal slewing rate with,

$$s_{int.} = \frac{2 I_{DS}}{C}$$

with typical values of 12 V/ μ sec resulting from $I_{DS} = 36 \mu A$ and $C = 6$ pF. The external slewing rate is set by the drain current of M12 with,

$$s_{ext.} = \frac{I_O(M12)}{C_L}$$

with typical values of 12 V/ μ sec resulting from $I_O = 300 \mu A$ and a load capacitance $C_L = 25$ pF, where $V^+ = +7.5V$ and $V^- = -7.5V$. Table 1 illustrates the design goals and performance obtained for the CMOS Operational Amplifiers.

Resistors R1, R2, R3, and R4 form a voltage-divider to set the output levels at the key nodes 5 and 6 in the circuit of figure 11. The significant feature of the design is that no ground (common) is present in the amplifier through which substantial current can flow and cause noise problems. A common-mode range of $\pm 1V$ requires M9 to remain in the pentode (saturation) region

when node 9 is at 5 V, while M8 and M12 must remain in saturation when nodes 9 and 12 reach -5 V. Since pentode or saturation requires,

$$V_{GS} - V_T \leq V_{DS}$$

when we have ± 7.5 V supplies and $V_{TN} = 1.3$ V, this means node 6 must be at 3.8 V and nodes 3, 4 and 5 must be at -3.8 V. The current sources M5 and M6 are biased by node 6 to minimize the

TABLE 1
CMOS OPERATIONAL AMPLIFIER $V^+ = +7.5$ V, $V^- = -7.5$ V

<u>Parameter</u>	<u>Design Goal</u>	<u>Measured</u>
Open Loop DC Gain	60 dB	70 dB
Unity Gain Frequency	1 MHz	2.0 MHz
Phase Margin	45°	45°
Slewing rate (+) ($C_L = 25$ pF.)	± 10 V/ μ sec	± 10 V/ μ sec
Off-set Voltage	< 20 mV	< 5 mV
Power Dissipation	15 mW	12 mW
Amplifier Size	200 mil ²	170 mil ²
Common-Mode Rejection	40 dB	50 dB
Common-Mode Range	± 5 V	± 5 V

number of bias settings required and are sized to meet the current requirements of the input and buffer stages. The geometry of the devices is set by the slewing rate requirements and desired power dissipation, within a specified amplifier size. Table 2 lists the W/L ratios for the transistors in the circuit of figure 17.

The open loop dc gain, phase margin, slew rate, etc., are all related to the compensation capacitor C which determines the stability of the amplifier. An analysis of the amplifier shown in figure 17a yields the open loop gain,

$$A_V(s) = \frac{A_V(0) \left[1 + sC/g_{m7} \right]}{1 + sC \left[\frac{A_V(0)}{g_{m1}} + R_{O4} + \frac{1}{g_{m7}} \right]} \quad (10)$$

where $A_V(0) = g_{m1}g_{m8}R_{O4}R_{O9}$ is the low-frequency dc open-loop gain, and the output impedances are,

$$R_{O4} = \frac{1}{g_{ds4} + g_{ds2}} \quad \text{effective output impedance at node 4} \quad (11)$$

$$R_{O9} = \frac{1}{g_{ds8} + g_{ds9}} \quad \text{effective output impedance at node 9}$$

For $A_V(0) \gg R_{O4} + 1/g_{m7}$, equation (10) reduces to

$$A_V(s) \approx A_V(0) \frac{(1 + sC/g_{m7})}{1 + sC A_V(0)/g_{m1}} \quad (12)$$

TABLE 2

(CMOS OPERATIONAL AMPLIFIER MOS TRANSISTOR W/L RATIOS)

<u>Transistor</u>		<u>Desired W/L Ratio (microns)</u>	<u>Mask W/L (microns)</u>
M1	M2	83/10	83/13
M3	M4	33/10	33/13
M5	M6	50/10	50/13
	M7	133/10	133/13
	M8	96/12	96/15
	M9	70/12	70/15
	M10	50/15	50/18
	M11	15/30	15/33
	M12	150/5	150/8
	Q13	Bipolar	Bipolar
	M14	50/15	50/18
	Q15	Bipolar	Bipolar

where the effect of the pole is minimized by maximizing g_{m1} and minimizing C subject to the constraints of bandwidth and slew rate. We note, the bandwidth and slew rate are given by,

$$\begin{aligned} BW &= g_{m1}/2\pi C \\ \text{Slew rate} &= 2I_{DS}/C \end{aligned} \tag{13}$$

and the transconductance of the MOS FET is related to the drain current by the expression,

$$g_{m1} = \frac{2I_{DS}}{V_{GS} - V_T} = 2 (\beta_o I_{DS})^{1/2} \tag{14}$$

which illustrates the interrelationship between the two quantities. The selection of g_{m7} is determined by the need to provide low output impedance and provide sufficient current for M7 so as not to limit the slew rate of the amplifier, while the channels of MOS transistors M8 and M9 must be selected to minimize output conductance (maximize output impedance R_{o9}).

The bipolar transistor Q_{13} can provide the necessary current for the positive slewing rate requirements; however, the current sink M12 must be selected to provide the necessary current for the negative slewing rate requirements. The feedback transistor Q_{15} limits the negative excursion on the base of Q_{13} to a diode drop below the output voltage. With this feature, the output voltage cannot overshoot on a negative slewing response and "lock" at the negative rail.

Table 2 indicates the final design W/L's for the various MOS Transistors; however, after the mask layouts were completed, the lengths were $3 \mu m$ oversize to allow for lateral diffusion and undercut during fabrication. Devices Q_{13} and Q_{15} are parasitic vertical NPN bipolar transistors formed in the p^- tub used for the N-channel MOS Transistors. Circuit simulation was performed with the ISPICE¹² Circuit Simulation Program and the device models

¹²ISPICE is a Circuit Simulation Program available from National, a division of CSC (Computer-Science Corporation), on time-share.

are shown in table 3, while the device sizes are shown in table 2.

With the device models of table 3 the CMOS amplifier shown in figure 17a was analyzed for small-signal, ac, frequency response. The transient response of a voltage follower was also simulated

TABLE 3
(ISPICE MODELING)

```
MODEL PMOS PDCM(VTO=1.3 PHI=.58 UD=220 NB=1E15 CO=3.4E-8%  
C1=6.8E-12 C2=6.8E-12 CRD=7.78E-12 CCB=7.78E-12 PB=.62 IS=1E-14%  
KN=.03 MN=1.0 KL=1.5 ECRIT=1.24E5 BETA=3.75E-6 GAMMA=.54%  
LAMBDA=1.15E-4)  
MODEL NMOS NSCM(VTO=1.3 PHI=.76 UD=550 NB=1.5E16 CO=3.4E-8%  
C1=6.8E-12 C2=6.8E-12 CRD=22E-12 CCB=22E-12 PB=.94 IS=1E-14%  
KN=.003 MN=1.58 KL=1.58 ECRIT=3.35E5 BETA=9.37E-6 GAMMA=2.1%  
LAMBDA=2.9E-5)
```

with the results for both simulations shown in table 4. The frequency response was examined for various compensation capacitors C and the transient response was simulated for a 5 V input step into a voltage follower, unity-gain, buffer amplifier driving a load capacitance of $C_L = 25$ pF.

A photomicrograph of the CMOS Operational Amplifier is shown in figure 17b. In the first mask designs, the compensation capacitor was made programmable with any combination of the values 1, 2, and 4 pF; however, based upon simulation (see table 3) a selection of 1 pF was used in the early fabrication runs. This was quite unfortunate, since the dc circuit simulation and experimental results agreed quite closely, while the ac circuit simulation was significantly different from the experimental measurements. The dc simulation and experimental results are illustrated in table 5.

The ac performance of the amplifier is critically dependent upon the output conductance modeling of the MOS Transistors and the capacitance modeling within the MOS Transistor. The 1 pF compensation capacitor, which was selected for the initial masks, was insufficient to achieve stable amplifier operation when the closed loop gain became less than 15 dB. Thus, with painstaking effort, an investigation was conducted to determine the necessary

TABLE 4
(ISPICE CMOS OPERATIONAL) AMPLIFIER SIMULATION
 $V^+ = +7.5V$ $V^- = -7.5V$ $C_L = 25$ pF

	Compensation Capacitance C pF)			
	4	2	1	0
Open-Loop Low Frequency Voltage Gain $A_V(0)$	63 dB			
Unity Gain Frequency (MHz)	2.15	3.83	4.65	11.0
Phase Margin	79°	68°	58°	22°
Gain Margin (dB)	-30	-25	-20	-10
Slewing rate (V/ μ sec)	22	25*	25*	25*

*Limited by external current supplied to load capacitance

TABLE 5
(DC SIMULATION AND EXPERIMENTAL MEASUREMENTS FOR CMOS OPERATIONAL AMPLIFIER: $V^+ = +7.5V$ $V^- = -7.5V$)

	<u>Simulated</u>	<u>Experimental</u>
Open-Loop DC Gain Voltage Gain $A_V(0)$	63 dB	65 - 70 dB
Input Off-Set Voltage V_{os} Referred to Input	0.4 mV (no mis-match assumed)	1 - 5 mV
Power Dissipation	16 mW	12 mW

modifications to achieve amplifier stability¹³. The result of these studies showed that an external 5 pF capacitor added to the internal 1 pF compensating capacitor and a 1 pF capacitor connected across the output of the high-gain inverter stage (i.e., from

¹³In a thesis by G. Smarandoiu, "Nonlinear Converters for Pulse-Code-Modulation Systems" College of Engineering, University of California, Berkeley, California, considerable SPICE simulation was performed on CMOS Buffer Amplifiers with $C = 10$ pF compensation capacitors.

node 9 to ground in figure 17a resulted in a stabilized amplifier. Table 6 illustrates the final ac results obtained for the stabilized CMOS Operational Amplifier. The small signal and large signal (transient step response) characteristics of the amplifier are illustrated in figure 18.

TABLE 6

(CHARACTERISTICS OF COMPENSATED CMOS OPERATIONAL AMPLIFIER

$C = 6 \text{ pF}$ $C_{9-0} = 1 \text{ pF}$ $V^+ = 7.5\text{V}$ $V^- = -7.5\text{V}$

Phase Margin	45°
Gain Margin	-12 dB
Settling Time (1.0%) 5 V Input Step $C_L = 5 \text{ pF}$	2 μsec
Slewing Rates	$\pm 10 \text{ V}/\mu\text{sec}$
Unity Gain Frequency	2 MHz

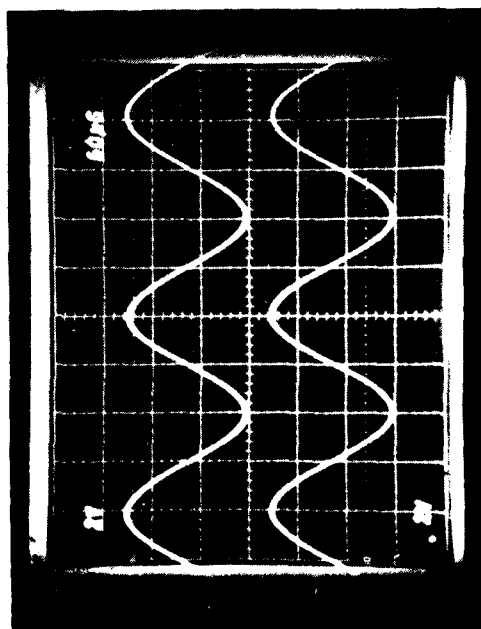
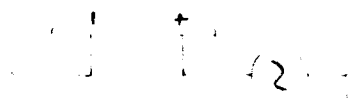


Figure 18. Voltage Follower Response

H. DIGITAL SHIFT REGISTER

Figure 19 illustrates the digital shift register which stores and shifts the sign of each data sample x_m in synchronism with its corresponding analog data sample in the CCD Analog Delay Line. The CMOS shift register is a dynamic shift register with a 2ϕ , non-overlapping, clocking scheme. The shift register is a serial-in/parallel-out (SI/PO) organization with the parallel output accomplished in a non-destructive manner. The parallel output represents the delayed data samples, x_{m-k} , required in the binary multiplication of the Exclusive OR circuit. Circuit operation is shown in figure 20.

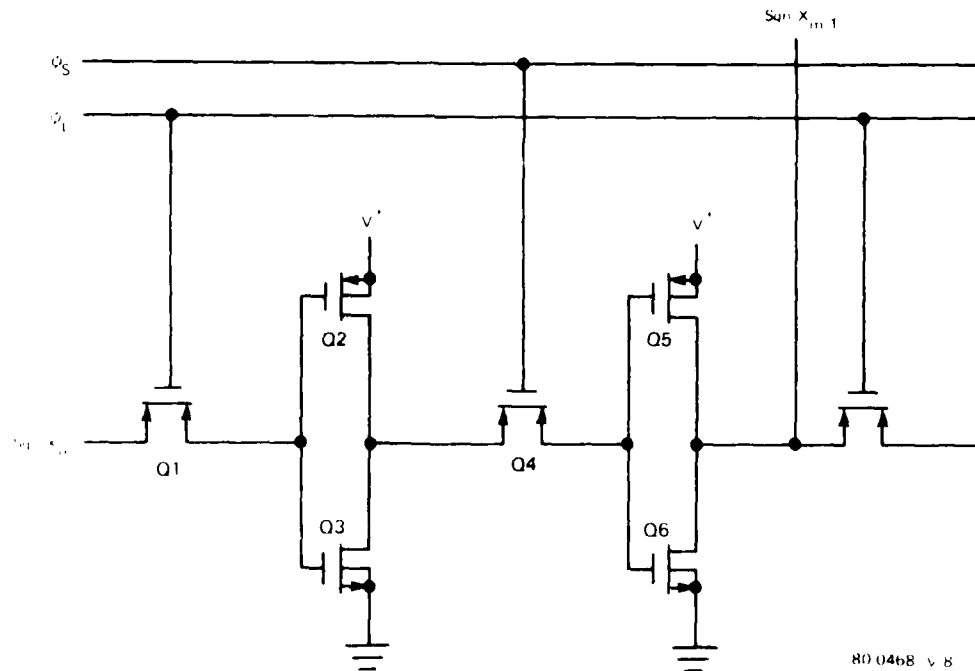


Figure 19a. Digital Shift Register

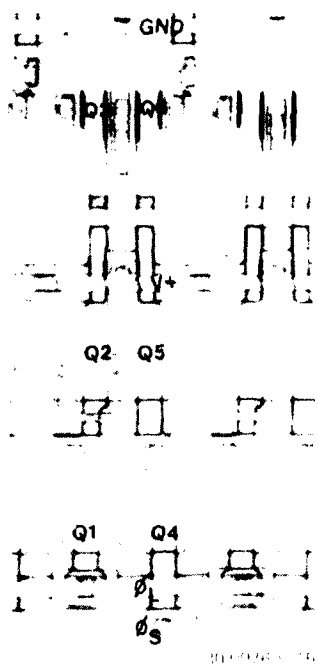
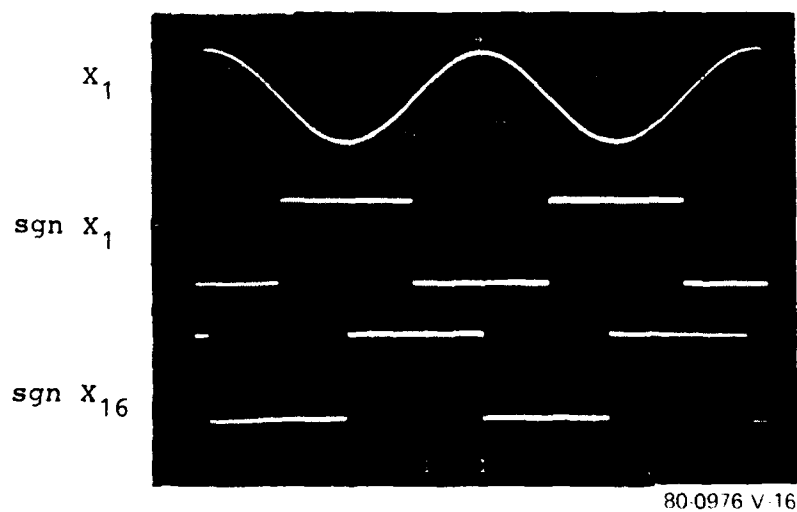


Figure 19b. Photomicrograph of Digital Shift Register Stage



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Figure 20. Shift Register Operation

I. EXCLUSIVE OR CIRCUIT

The Exclusive OR Circuit, illustrated in figure 21a, forms the binary multiplication product,

$$\begin{aligned}
 \text{sgn}(x_{m-k}) \oplus \text{sgn}(e_m) &= \text{sgn}(x_{m-k}) \overline{\text{sgn}(e_m)} \\
 &\quad + \overline{\text{sgn}(x_{m-k})} \text{sgn}(e_m) \\
 &= 1 \text{ sgn}(x_{m-k}) \neq \text{sgn}(e_m) \\
 &= 0 \text{ sgn}(x_{m-k}) = \text{sgn}(e_m)
 \end{aligned}
 \tag{15}$$

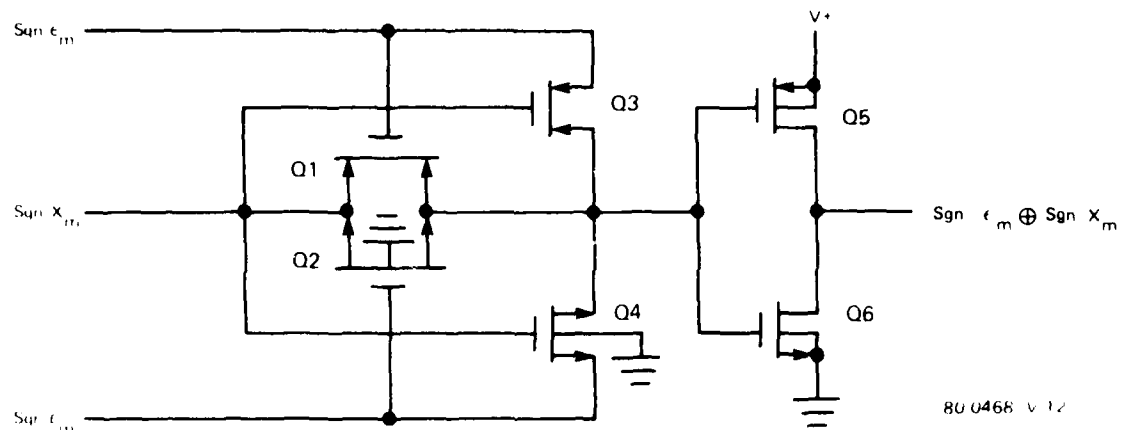
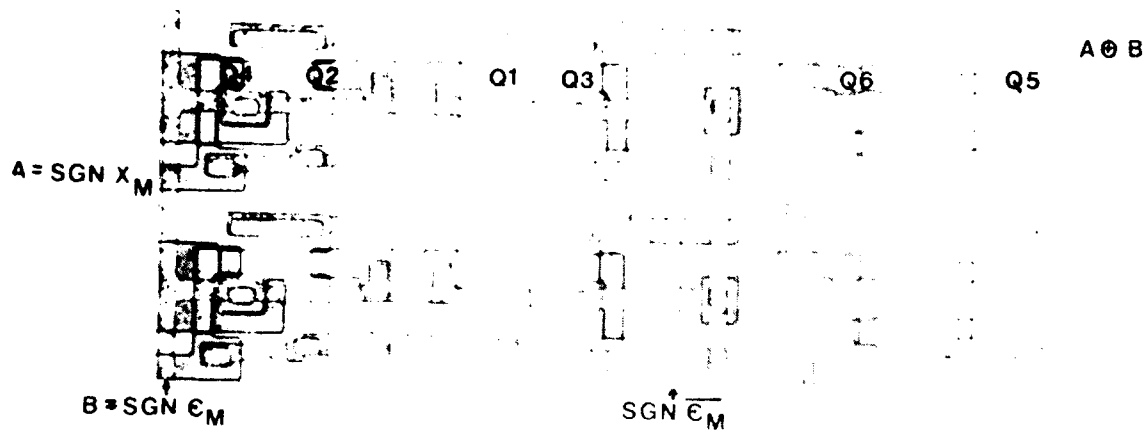


Figure 21a. Exclusive OR Circuit

A "1" state produces a weight increment, while a "0" state produces a weight decrement. A photomicrograph of the Exclusive OR stage is illustrated in figure 21b and the operation of the circuit is shown in figure 22.

J. LEVEL SHIFTER CIRCUIT

The 0 to +7.5 V output of the Exclusive OR Circuit is level-shifted to a -7.5 V to +7.5 V output such that the steering network, a "double-pole/double-throw" switch, may be operated in a manner to accept analog signals which vary around ground.



80-0976-V 17

Figure 21b. Photomicrograph of Exclusive OR Stage

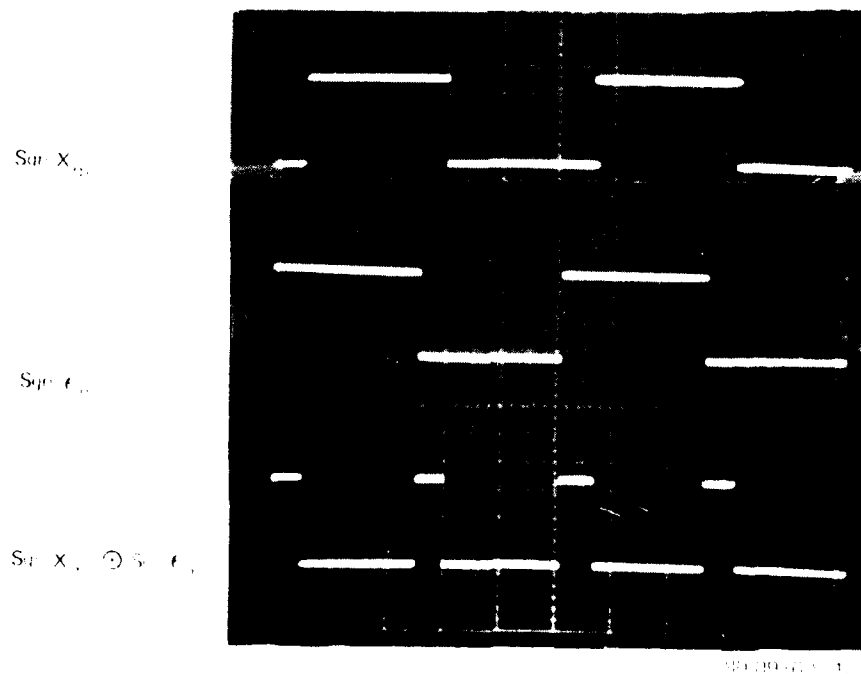


Figure 22. Exclusive OR Circuit Operation

The circuit which accomplishes this function is a cross-coupled, flip-flop and is illustrated in figure 23a. This circuit performs the level-shifting function with the address of the PMOS Transistors. The operation requires the proper ratioing of $(W/L)_p/(W/L)_n$, which is typically 15/1 to ensure regenerative action occurs. A photomicrograph of the level-shifter is shown in figure 23b.

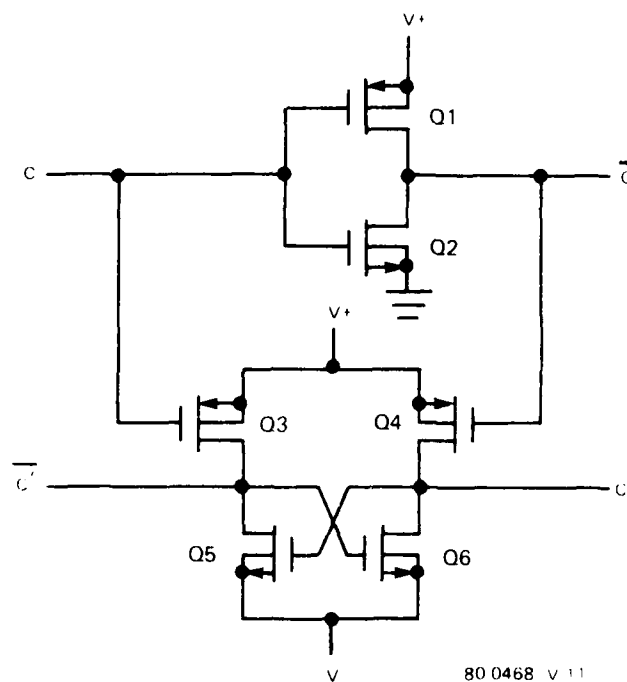


Figure 23a. Level Shifter Circuit

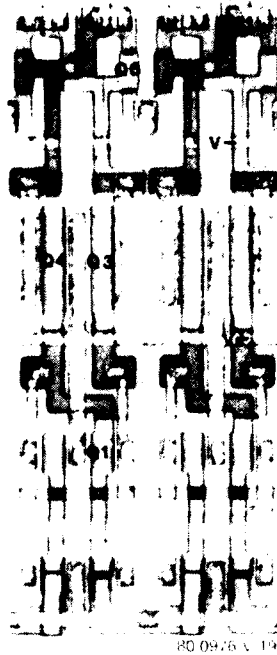


Figure 23b. Photomicrograph of Level Shifter

K. STEERING NETWORK

The steering network acts as a "double-pole/double-throw" switch to apply the appropriate signals to the bidirectional charge-control (BC^3). A schematic of the steering network is illustrated in figure 24a while a photomicrograph is shown in figure 24b. The input signals to the steering network are IG_p and $2\mu e_o$, where the former is a digital signal with a 15 V excursion, and the latter is an analog signal. From figure 24a, the output signals $P\phi_{G1}$ and $P\phi_{G3}$ are controlled with the level shifter outputs as follows:

$$\begin{aligned}
 P\phi_{G1} &= 2\mu e_o & \text{for } C' = +V \\
 &= IG_p & \text{for } C' = -V \\
 P\phi_{G3} &= IG_p & \text{for } C' = +V \\
 &= 2\mu e_o & \text{for } C' = -V
 \end{aligned}
 \tag{16}$$

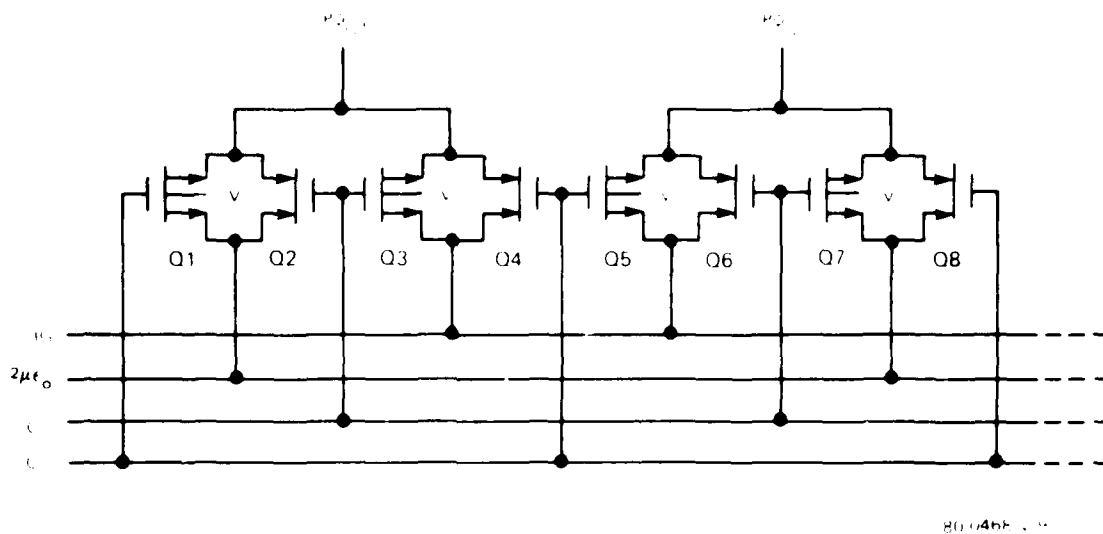


Figure 24a. Steering Network

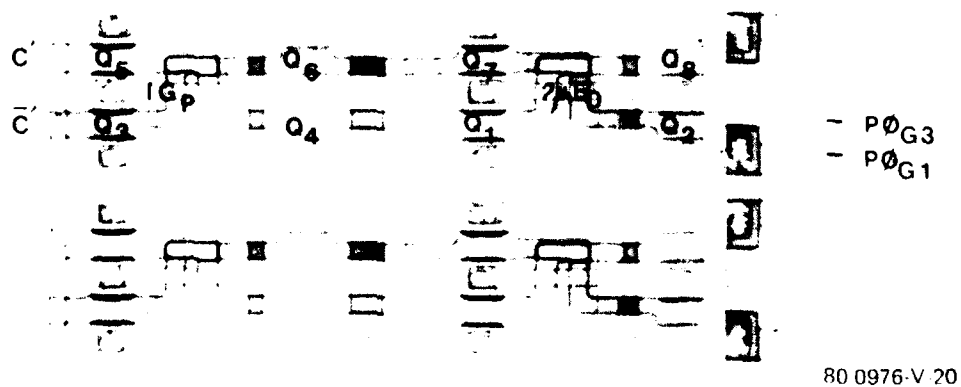


Figure 24b. Photomicrograph of Steering Network

L BIDIRECTIONAL CHARGE CONTROL CIRCUIT

The bidirectional charge control circuit (BC^3), illustrated in figure 25 along with the MOS transistor weights, changes the value of the programmable analog conductance at the respective tap location. The circuit uses the principle of stabilized charge injection to perform the weight change. The signals designated $P\phi_{G1}$ and $P\phi_{G3}$ are derived from the output of the steering network. The BC^3 performs both an increment and decrement operation as determined by the output of the Exclusive OR Circuit at each tap location.

Figure 26 illustrates a cross-section of the BC^3 , the potential profiles, and the required timing to increment the conductance (weight) of the MOS multiplier. To increment a tap weight requires 6 distinct time intervals. The function of each time interval is as follows:

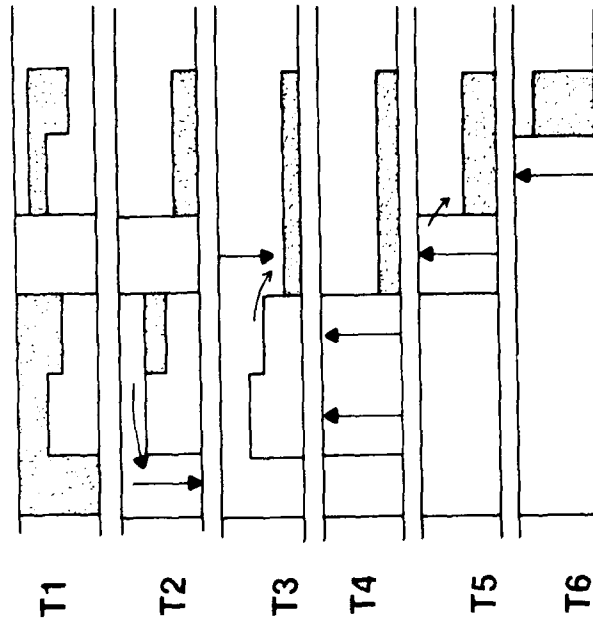
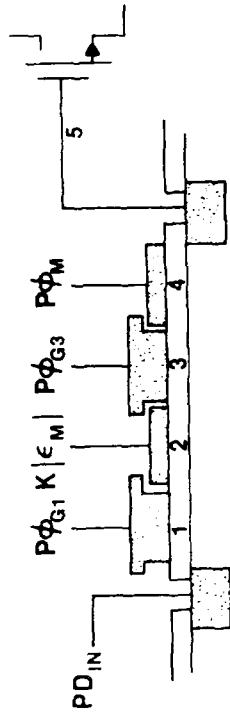
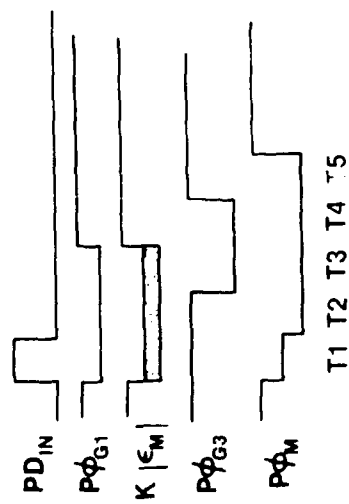
$t = t_1$:

1. PD_{in} pulses to substrate, filling the potential wells under electrodes 1 and 2 with minority carriers.
2. $P\phi_M$ is pulsed to ground and the charge on the gate of the MOS transistor weight becomes shared between the potential wells under electrodes 4 and 5.

$t = t_2$:

1. PD_{in} pulses to V_- (-7.5 volts) causing the PD_{in} electrode to become a drain for the excess minority carrier charge under electrodes 1 and 2. The charge remaining under electrode 2 after stabilization is given by:

$$Q_s = C_2 (K |\epsilon_m| - P\phi_{G1})$$



78-0559-8B-7-1

Figure 26. Bidirectional Charge Control Circuit (BC^3) Weight Increment

where

- Q_S = signal charge to be injected into CCD
- C_2 = effective capacitance of electrode 2
- $P\phi_{G1}$ = voltage on electrode 1 during the stabilization period
 $\cong 0$ volts
- $K |\epsilon_m|$ = voltage on electrode 2 during the stabilization period
- 2. $P\phi_M$ pulses to -7.5 volts resulting in a further charge redistribution between the potential wells under electrodes 4 and 5.

$t = t_3$:

- 1. $P\phi_{G3}$, the injection gate signal, pulses to -7.5 volts causing the charge initially shared between electrodes 4 and 5 to become shared between electrodes 3, 4, and 5.
- 2. The signal charge under electrode 2 is added to the charge under electrodes 3, 4, and 5.

$t = t_4$:

- 1. Electrodes 1 and 2 are pulsed to substrate, isolating the PD_{in} electrode from the injection gate electrode.

$t = t_5$:

- 1. Electrode 3 (injection gate) is pulsed to substrate, forcing all charge to be shared between electrodes 4 and 5.

$t = t_6$:

- 1. $P\phi_M$ pulses to substrate, forcing all charge (original charge plus increment) onto the capacitance associated with the gate electrode of the MOS transistor weight.

Figure 27 illustrates a cross section of the electrode configuration, potential profiles, and the required timing to decrement the conductance of the MOS transistor weight. The weight decrement configuration is achieved by using the weight increment

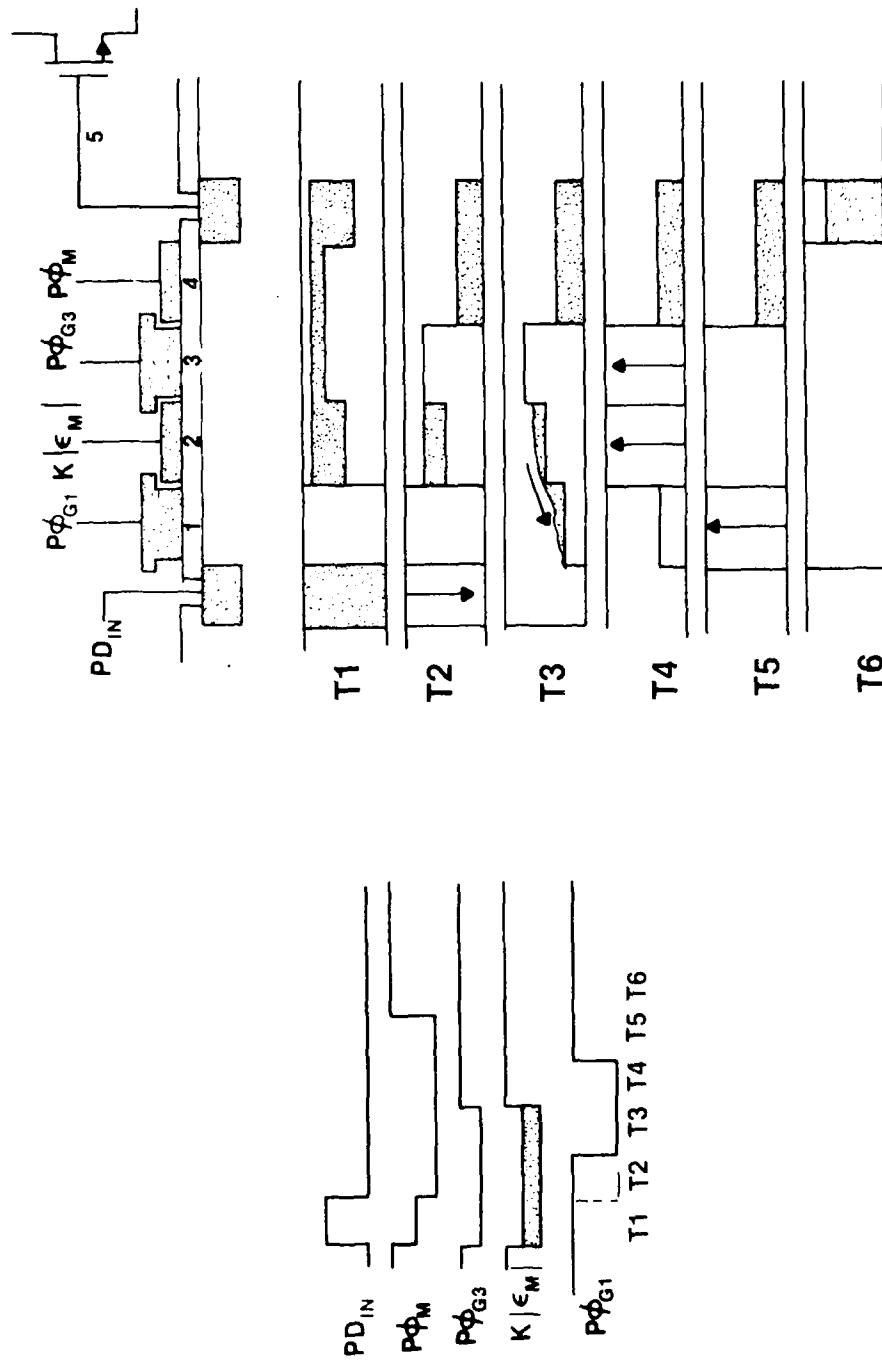


Figure 27. Bidirectional Charge Control Circuit (BC³) Weight Decrement

configuration and interchanging the signals on electrodes 1 and 3. The electrode signal interchange is performed by the steering network.

The weight decrement operation also requires six distinct timing intervals. Referring to figure 27, the operation of the BC^3 in the decrement cycle is as follows:

$t = t_1$:

1. $P\phi_M$ pulses to ground and causes the charge, initially stored on the capacitance associated with the gate electrode of the MOS transistor weights, to be shared between electrode 5, 4 (nominally at ground potential), and 2, which is below ground potential by $K |\epsilon_m|$.

$t = t_2$:

1. $P\phi_M$ pulses to -7.5 volts, causing electrode 4 to act as a drain for the excess charge under electrodes 2, 3, 4, and 5. A quantity of charge given by

$$Q_S = C_2 K |\epsilon_m|$$

is removed from the initial gate charge of the MOS transistor weight.

$t = t_3$:

1. The injection gate pulse in electrode 1 is enabled and the charge under electrode 2 is injected into the input diode at a potential of -7.5 volts.

$t = t_4, t_5$:

1. Electrodes 1, 2, and 3 are pulsed to substrate, which isolates the gate of the MOS weight from the input diode.

$t = t_6$:

1. $P\phi_M$ is pulsed to substrate and all remaining charge is injected onto the capacitance associated with the gate of the MOS weight.

Figure 25b is a photomicrograph of the BC^3 circuit and MOS weights while figure 28 shows operation of the circuit as an integrator.

With the weight change by the BC^3 discussed, the final parameter which enters into the "clipped data" LMS algorithm

$$W_k(m+1) = W_k(m) + 2\mu \cdot \text{sgn } x_k \cdot \text{sgn } \epsilon_{(m)} \cdot |\epsilon_{(m)}|$$

is determination of the convergence factor μ . For the values of the resistors used on the chip, the size of the MOS weight transistors, and electrode capacitance of the BC^3 , μ is given by (see Appendix A)

$$\mu = 4.68 \times 10^{-5} R_{EXT}$$

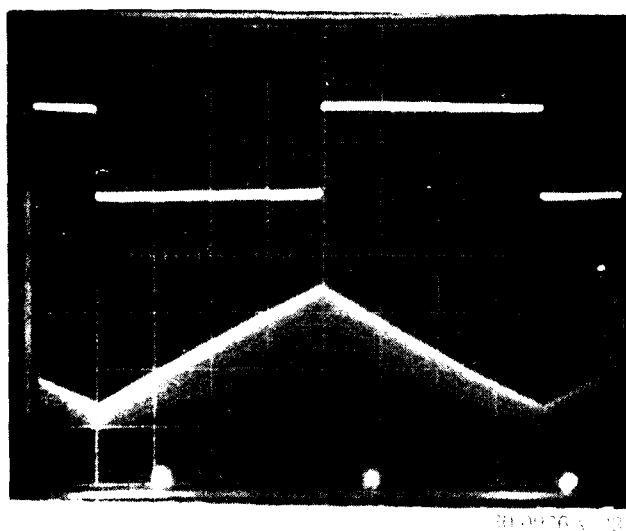


Figure 28. Bidirectional Charge Control Circuit Operation as a Dual-Slope Integrator

CHIP TIMING AND CLOCK GENERATION CIRCUITRY

Figure 29 illustrates the digital waveforms required to clock the circuits on the adaptive filter chip. The thirteen waveforms can be divided into 3 groups: one group to clock the CCD, a second group to control the analog signal processor and digital shift

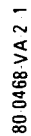


Figure 29. 7012 Unified Timing Diagram

register, and a third group to clock the bidirectional charge control circuits. The CCD timing and clamp/sample cycle are designed to maximize the time available for weight update in order to minimize the constraints on the operational amplifiers. In addition, the timing is designed to minimize the complexity of the combinatorial logic timing generator circuitry.

Figure 30 shows the timing waveforms as obtained from the chip. Considerable loading effects are due to probing with a high capacitance probe. All waveforms are correct except for $P\phi_{MH}$ which has been corrected by a mask change.

A schematic of the timing generator is shown in figure 31. The input clock is counted down by 3 D-type flip-flops. Outputs are taken from the master (M, \bar{M}) and slave (Q, \bar{Q}) of each flip-flop and are used in conjunction with nand-gate combinatorial logic to generate the required waveforms. All the combinatorial logic functions are performed at low logic levels (0 to +7.5 V) and translated to high logic levels (-7.5 V to +7.5 V) by level shifters to reduce power dissipation. ISPICE simulations were used to size the devices to achieve 100 nsec rise and fall times on all clock waveforms.

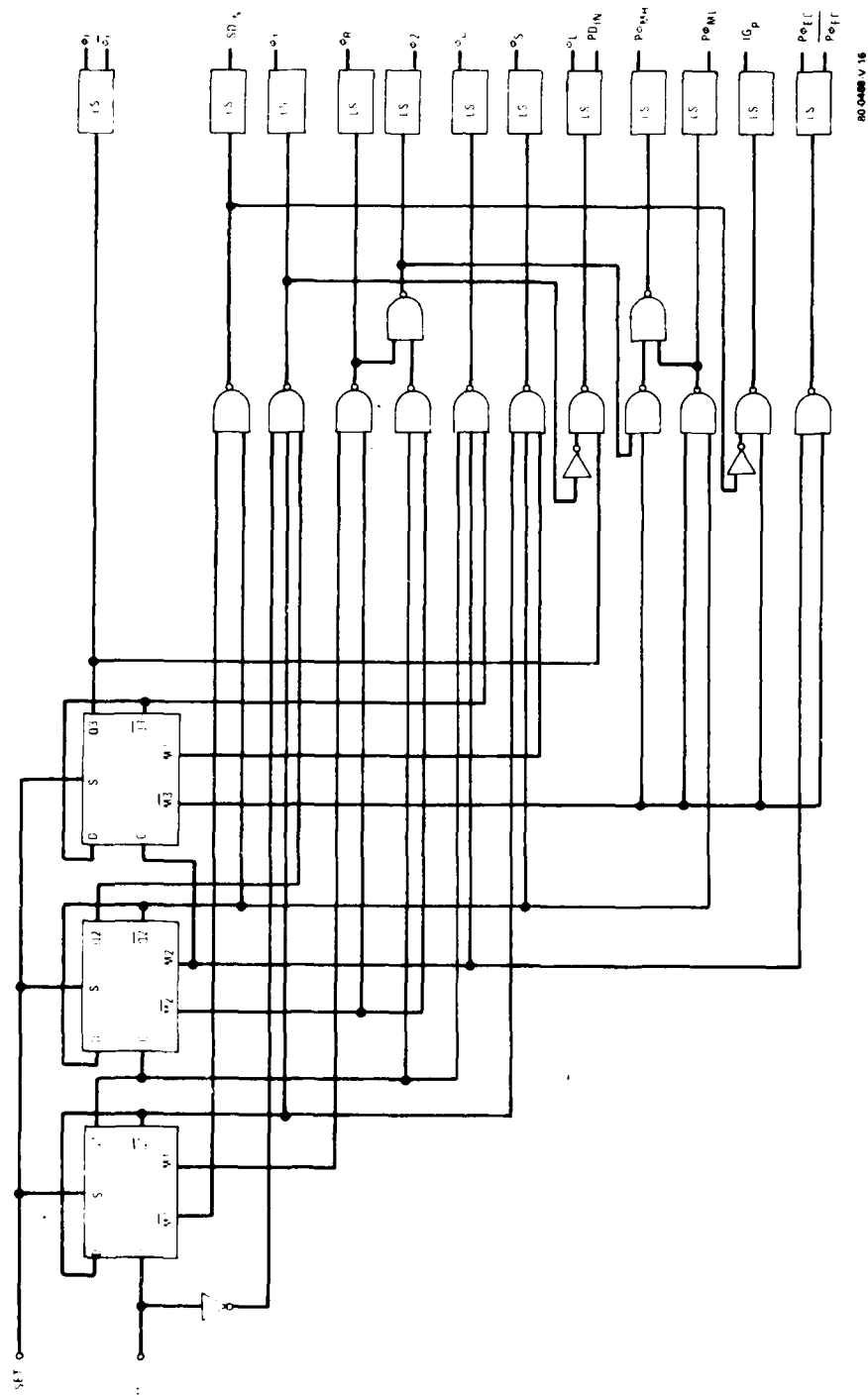


Figure 31. Timing Generator Schematic

FEATURES OF THE MONOLITHIC ADAPTIVE FILTER

Figure 32 shows a complete schematic of the adaptive filter and several features are included which have not been discussed. The first feature is the ability to externally program the tap weights. External programming is enabled by bringing the voltage designated V_M to +7.5 volts and V_{WR} to -7.5 volts. This action disables $\text{sgn } x_m$ from entering the digital shift register and enables the weight commutation transistor, respectively. An external strobe pulse, SR_I , is entered into the shift register and the external analog weight, W_{EXT} , is transmitted onto the gate of the MOS transistor weight when the shift register pulse enables the respective p-channel commutation transistor via the steering network. The external update mode automatically disables the BC^3 output at each tap location. As the weight update is sequential in the external mode, a lower limit is placed on the shift register scan rate and weight refresh time due to the retention time of the charge on the gate of the MOS transistor weight.

The second feature included on the adaptive filter chip is the ability to interrogate or read out the weight values. With V_{WR} and V_M at +7.5 volts, impulsing the CCD will produce an output response, y_m , which is a linear function of the weight value at each tap location. These weight values can then be stored, if desired, and reprogrammed via the technique just discussed to form a filter with a fixed impulse response.

An additional feature is the ability to use the error derived internally via

$$\epsilon_m = d_m - y_m$$

or have the error derived externally from a process, for instance, not explicitly connected with the reference input. Shorting the two bonding pads labelled $\textcircled{\text{CAS}}$ causes the internally generated error to be used.

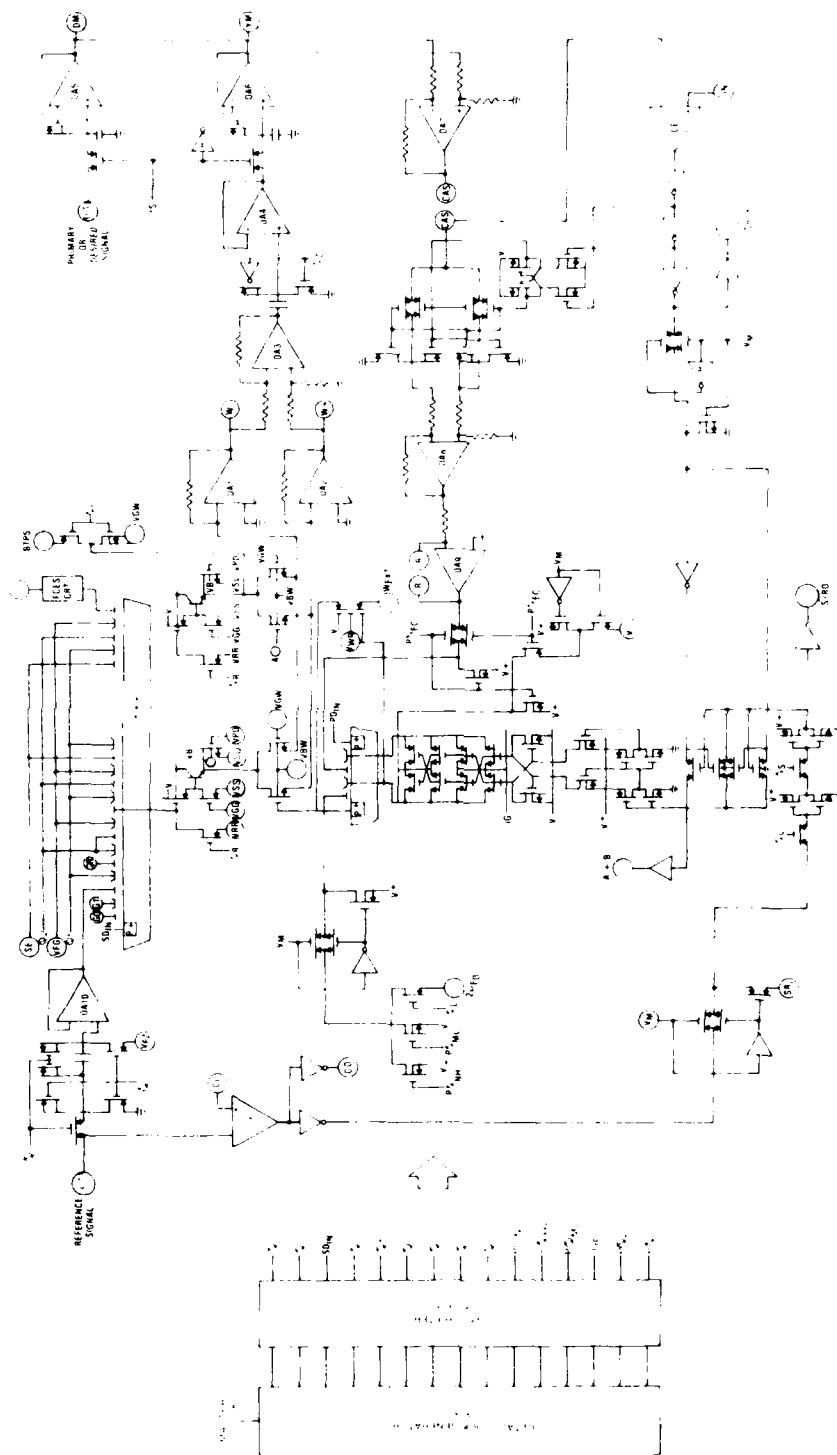


Figure 32. Schematic of Adaptive Filter

An additional tap called the "bias tap" is included on the chip to compensate for slow variations in the dc level of the desired input signal. Finally, the adaptive filter chip is designed such that chips can be cascaded to form adaptive filters requiring a larger number of taps.

IV. FABRICATION TECHNOLOGY

The CCD Adaptive Signal Processor is fabricated with an ion-implanted, double polysilicon, CMOS technology. Figure 33 illustrates the process sequence employed in the fabrication of the Adaptive Filter chip. There are basically 10 photosteps including protective silox overcoat for the bonding pads. A cross-section of the CCD Adaptive Filter is illustrated in figure 34. The first ion-implantation is used to define the p^- well for the NMOS Transistors, while the second ion-implantation determines the sheet resistance of the resistors for the CMOS Operational Amplifiers. The basic gate insulator is a dual dielectric consisting of 800 Å SiO_2 covered with 500 Å of Si_3N_4 . The gate electrodes are phosphorous-doped, polysilicon and the CCD is a double polysilicon, coplanar, electrode geometry. Several unique features of this design are the ion-implanted resistors, the field shield to prevent field inversion, and the double polysilicon capacitor which is used for the compensation and clamp/sample capacitors. An important step in the overall process is the so-called "back-side" getter to sink the dislocations and provide excellent bulk lifetimes. Table 7 illustrates some of the process parameters obtained in the CCD CMOS Technology.

The surface recombination velocity is minimized with a H_2 anneal after the contact windows are opened in step (34). The sheet resistance versus channel length is illustrated in figure 35 and the nominal value used in the process is 1000 Ω/square for an ion-implantation of $1 \times 10^{13} \text{ ions/cm}^2$ at $E = 80 \text{ KeV}$ (Boron). The linearity and stability of the ion-implanted Boron resistors is excellent. Typical C-V characteristics for the CMOS process are illustrated in figure 36 and the I-V characteristics of minimum

MATERIAL: N-TYPE (100), 4-8 OHM-CM., FZ, WACKER

- | | |
|---|--|
| (1) 6kA ⁰ INITIAL OXIDATION (STEAM 1000°C) | (21) 500A ⁰ Si ₃ N ₄ DEPOSITION (750°C) |
| (2) #1-PHOTOSTEP (7012-1) P ⁻ WELL | (22) POLYSILICON DEPOSITION 5kA ⁰ |
| (3) 500 A ⁰ OXIDE (DRY HCL 1000°C) | (23) PHOSPHOROUS DOPE POLY-Si (950°C, 15MIN.) |
| (4) ION-IMPLANTATION (BORON) E=80KEV, Ø=1.7x10 ¹³ CM ⁻² | (24) 3kA ⁰ SILOX MASKING OXIDE |
| (5) DRIVE-IN (24 HRS. @ 1150°C) | (25) #5-PHOTOSTEP (7012-6B) POLY-Si 1 |
| (6) 6kA ⁰ OXIDATION (BACK-SIDE PROTECT) | (26) 2kA ⁰ OXIDE (STEAM, 1000°C, STRIP SILOX) |
| (7) #2-PHOTOSTEP (7012-3A) N ⁺ AND P ⁺ DIFFUSIONS | (27) POLYSILICON DEPOSITION 4.5kA ⁰ |
| (8) 300 A ⁰ OXIDE (1000°C) | (28) PHOSPHOROUS DOPE POLY-Si (950°C, 15MIN.) |
| (9) Si ₃ N ₄ DEPOSITION 1.6kA ⁰ (750°C) | (29) 5kA ⁰ SILOX MASKING OXIDE |
| (10) #3-PHOTOSTEP (7012-4A) P ⁺ DIFFUSION | (30) #5-PHOTOSTEP (7012-7) POLY-Si 2 |
| (11) BORON DIFFUSION (150 OHM/SQUARE, 1000°C) | (31) 1.1kA ⁰ OXIDE (STEAM, 900°C, STRIP SILOX) |
| (12) Etch Si ₃ N ₄ AND SiO ₂ (THIN) | (32) #7-PHOTOSTEP (7012-8POS.) CW-DIFFUSION |
| (13) PHOSPHOROUS DIFFUSION (10 OHM/SQUARE, 900°C) | (33) 7kA ⁰ SILOX DENSIFIED (900°C, 20MIN.) |
| (14) 800 A ⁰ OXIDE (STRIP ORIGINAL OXIDE) | (34) #8-PHOTOSTEP (7012-9) CW-DIFFUSION & POLY |
| (15) #4-PHOTOSTEP (7012-5A) P ⁻ RESISTOR IMPLANT | (35) H ₂ ANNEAL, 60 MIN @ 500°C |
| (16) ION-IMPLANTATION (BORON) E=80KEV, Ø=3x10 ¹³ CM ⁻² | (36) ALUMINUM DEPOSITION 10kA ⁰ (AL-Si) |
| (17) 10-A ⁰ SILOX FRONT SURFACE PROTECT | (37) #9-PHOTOSTEP (7012-10A) AL INTERCONNECT |
| (18) PHOSPHOROUS SETTER (30MIN, 1050°C) | (38) SINTER 500°C (50% H ₂ , 50% N ₂) 25 MIN. |
| (19) 15kA ⁰ SILOX BACK SURFACE PROTECT | (39) SILOX (4.5kA PHOS. DOPED+ 4.5kA ⁰ UNDOPED) |
| (20) 8000A GATE OXIDE (DRY HCL, 900°C) | (40) #10-PHOTOSTEP (7012-11) BONDING PADS |

Figure 33. CCD Adaptive Filter Processing Sequence

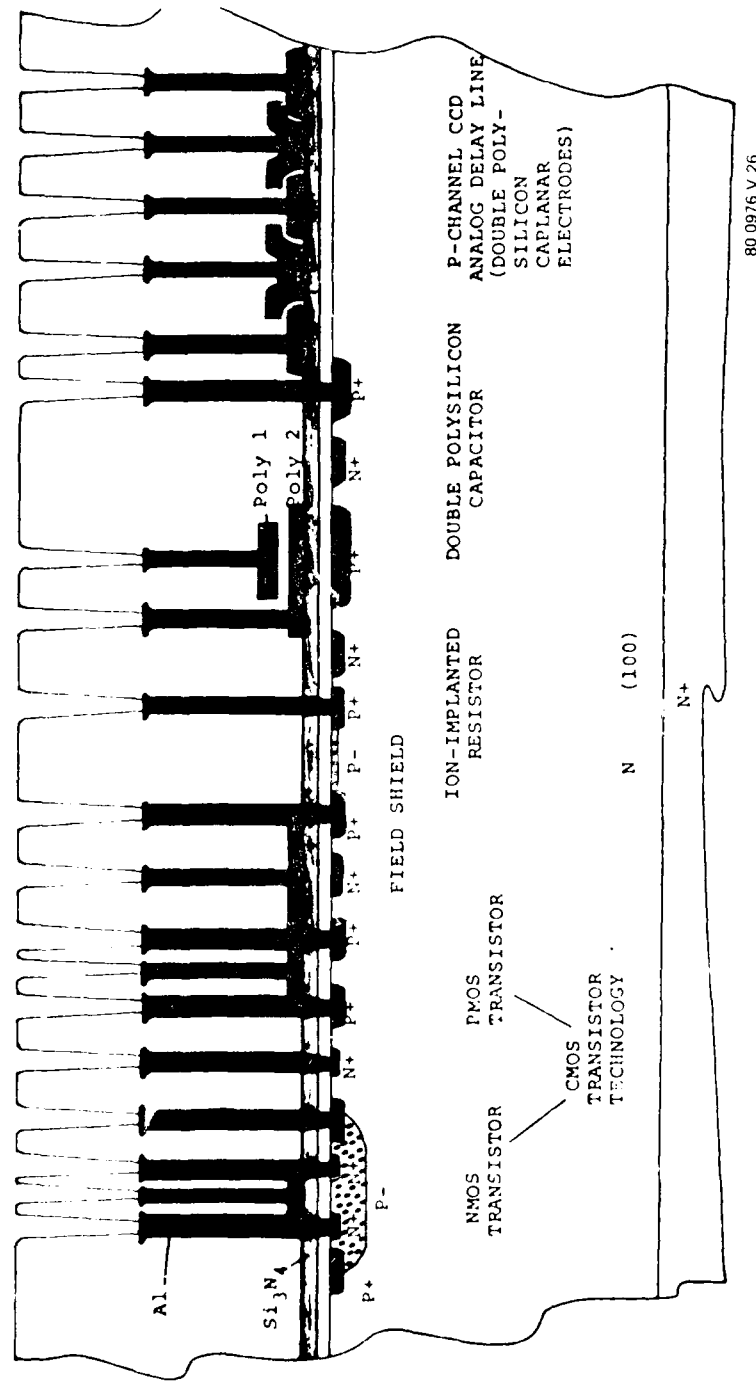
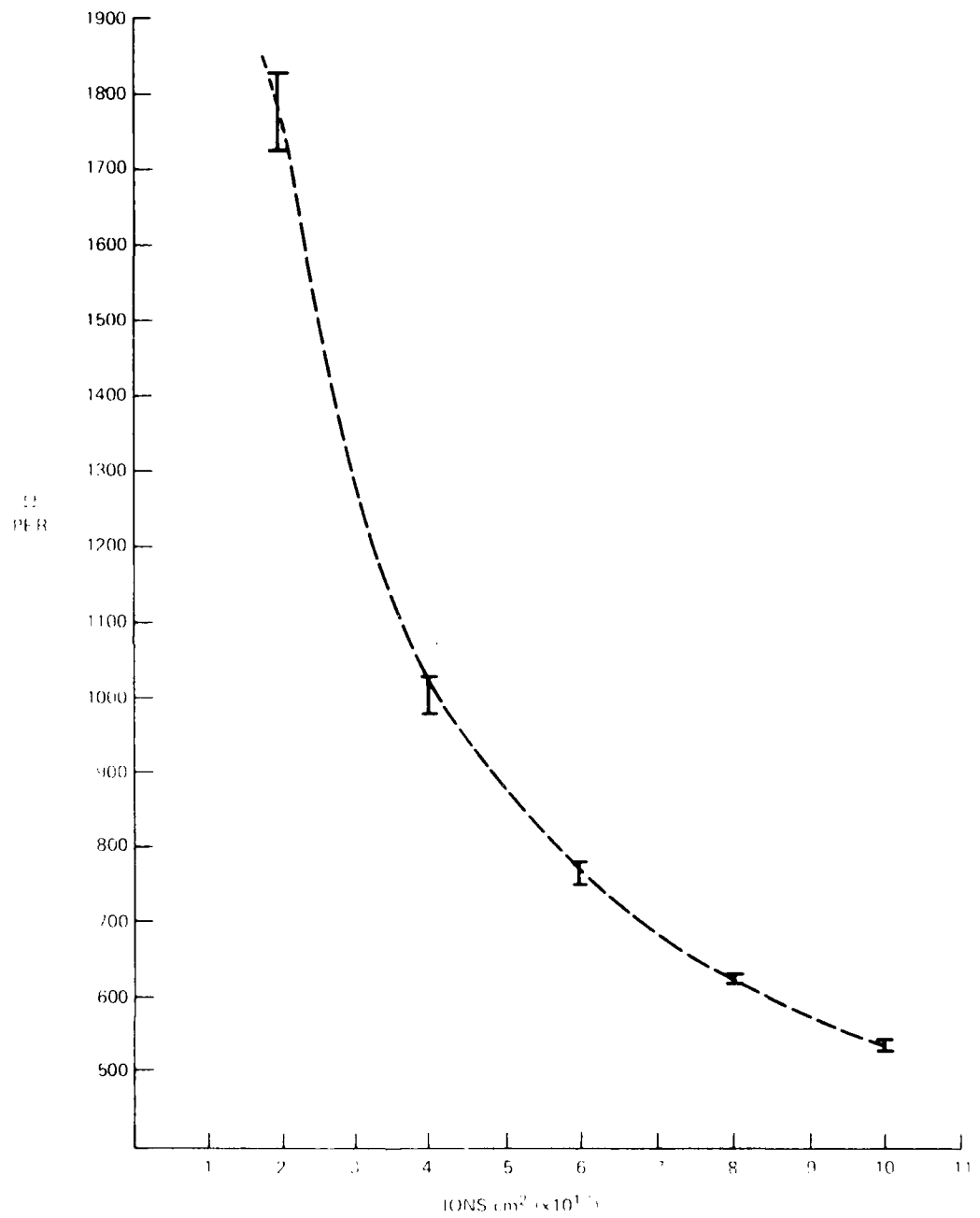


Figure 34. CCD Adaptive Filter Technology Cross-Section

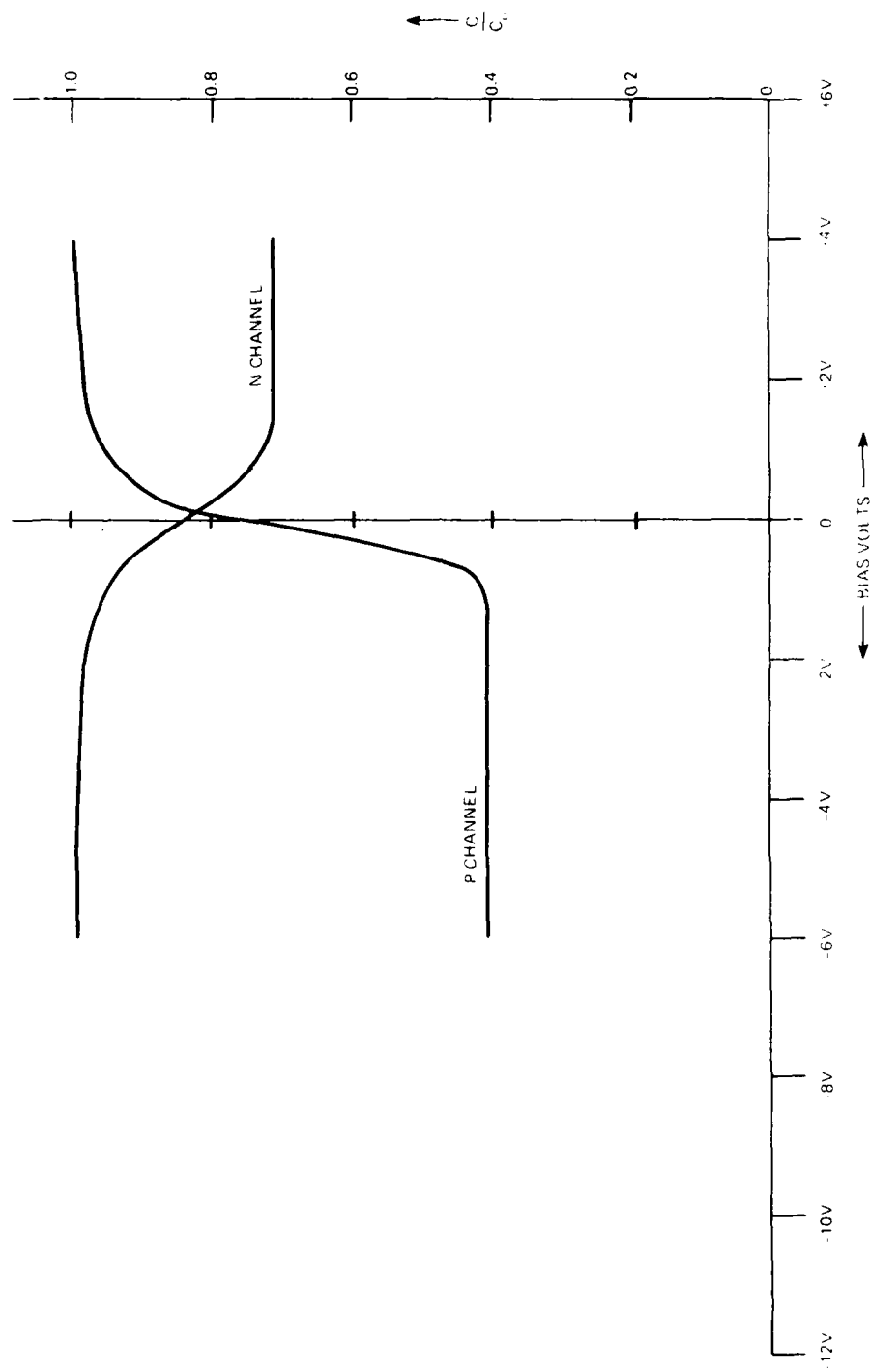
TABLE 7
(CCD/CMOS PROCESS PARAMETERS)

Threshold Voltage		
P-channel MOSFET		-1.6 to -2.1 V
N-channel MOSFET		0.8 to +1.6 V
Breakdown		
P ⁺ to N		45 V
N ⁺ to P ⁻		24 V
P ⁻ to N		250 V
Substrate NPN Bipolar Transistor		
β ($I_C \approx 1$ mA)		100 - 150
BV _{CEO}		60 V
Minority Carrier Generation- Recombination Lifetimes (C-t)		100 μ sec



80 09 56 V 27

Figure 35. Boron Implant Sheet Resistance
Versus Implant Dosage



20 09 76 V 28

Figure 36. Threshold Voltages for 7012 CMOS Process

geometry PMOS and NMOS Transistors are shown in figure 37. Figure 38 illustrates the I-V characteristics of the Substrate NPN Bipolar Transistor, which is used in the CMOS Operational Amplifiers and the FCES circuit at each tap position of the CCD analog delay line. Figure 39 illustrates a C-V characteristic of a PMOS capacitor and a C-t curve which illustrates a high bulk lifetime in excess of 350 μsec . This is due to the excellent bulk gettering with phosphorous and the front-surface anneal with hydrogen. The leakage current for the CMOS process is typically 10 nA/cm².

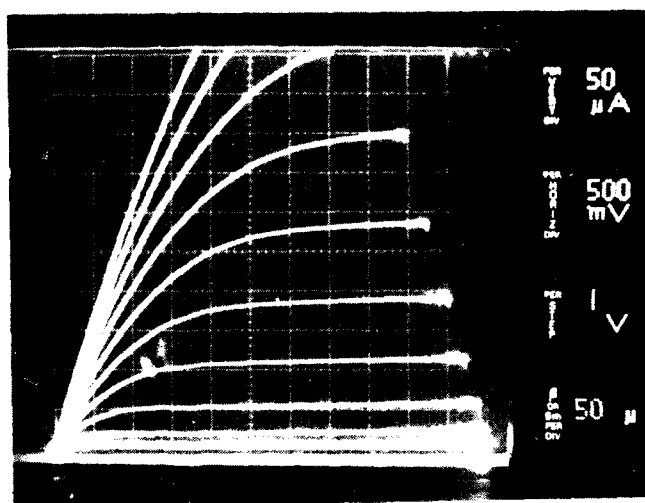
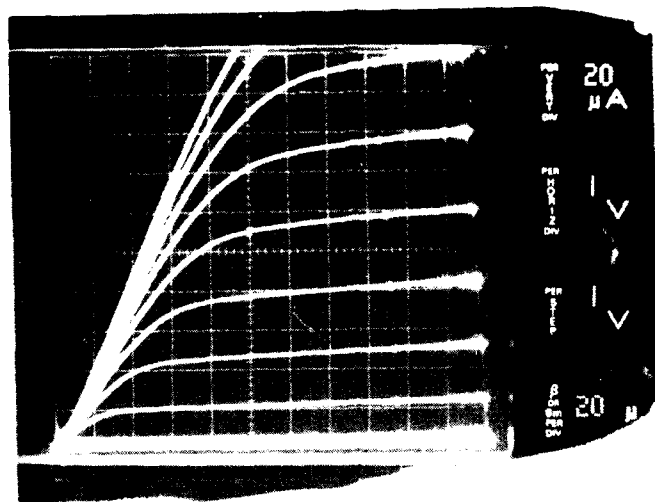
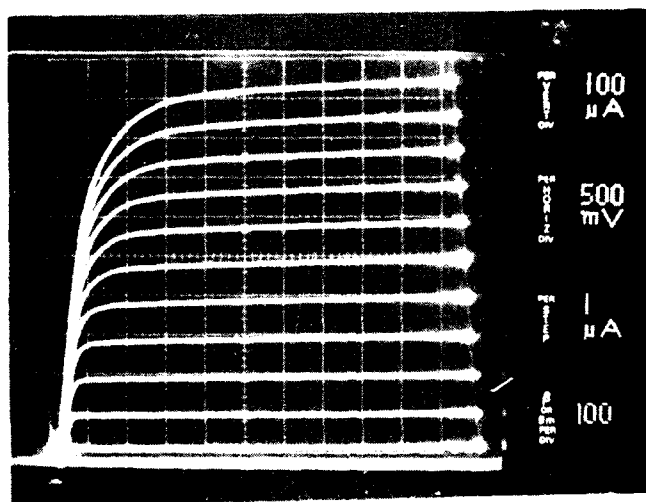


Figure 37a. I-V Characteristic of N-Channel MOSFET (Low Voltage)



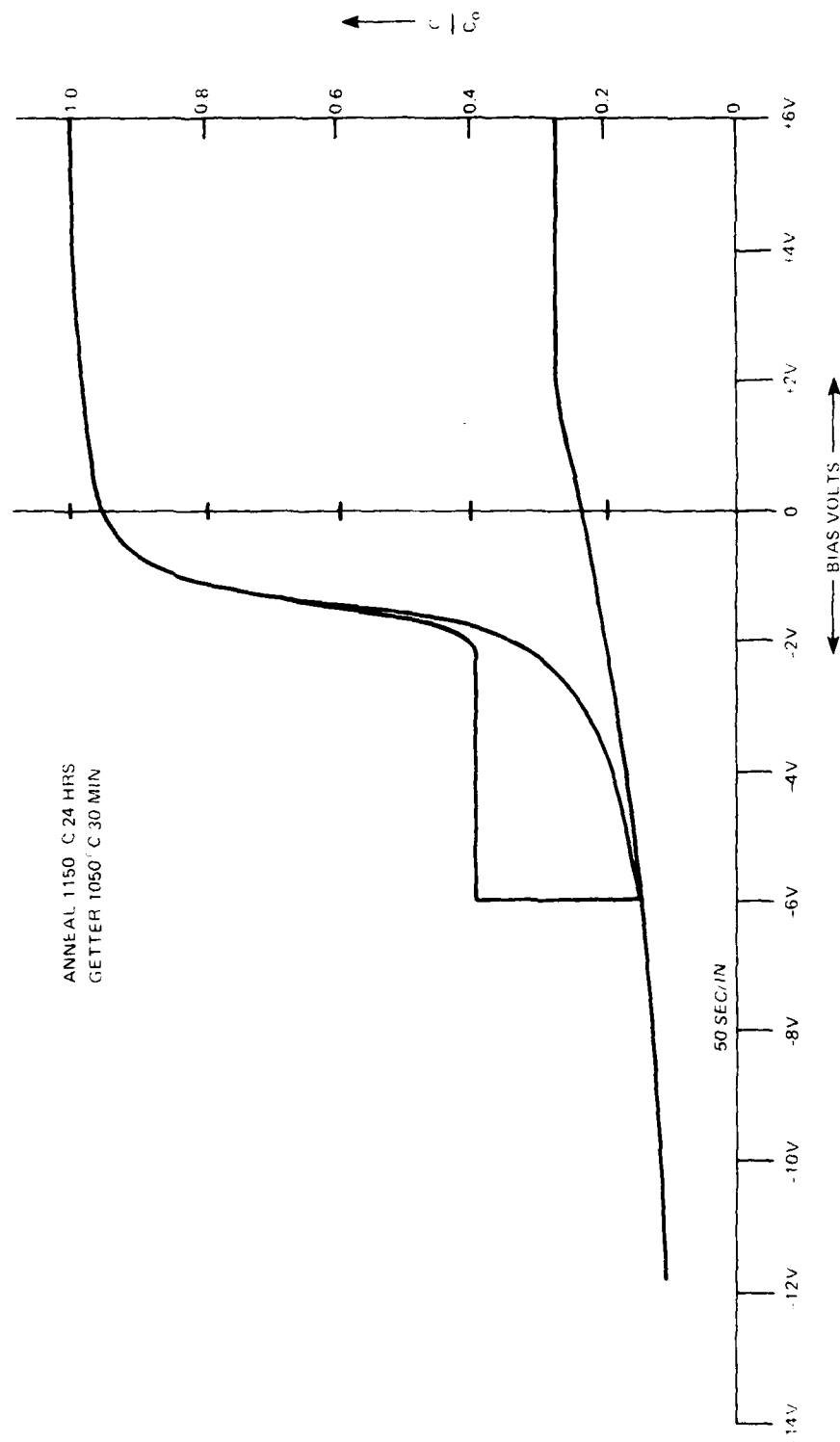
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Figure 37b. I-V Characteristic of P-Channel MOSFET



51

Figure 38. I-V Characteristics of the NPN Bipolar Transistor



80 0976 V 31

Figure 39. C-t Measurement of Lifetime

The electrode structure of the CCD is an overlapping, dual polysilicon, co-planar, geometry as illustrated in the cross-section of figure 34. A Scanning Electron Microscope (SEM) view of the CCD structure is illustrated in figure 40(a) and 40(b) with the low-temperature silox overcoat and insulating thermal oxide between the two polysilicon layers clearly visible. The $2\text{ }\mu\text{m}$ overlap of the polysilicon electrodes is visible in figure 40(b), which was taken of a cross-section of the CCD analog shift register.

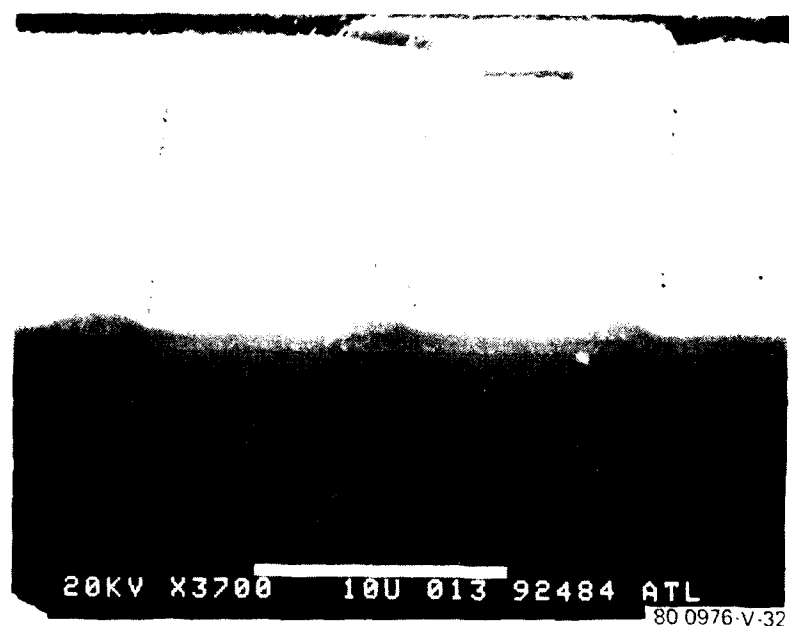


Figure 40a. Top View of CCD Analog Shift Register
(Delay Line) With Electrode Length = $7\text{ }\mu\text{m}$
and Width = $125\text{ }\mu\text{m}$

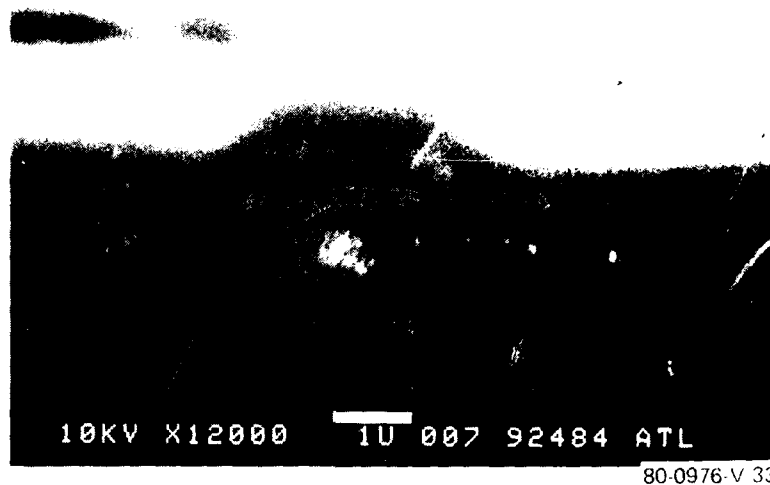
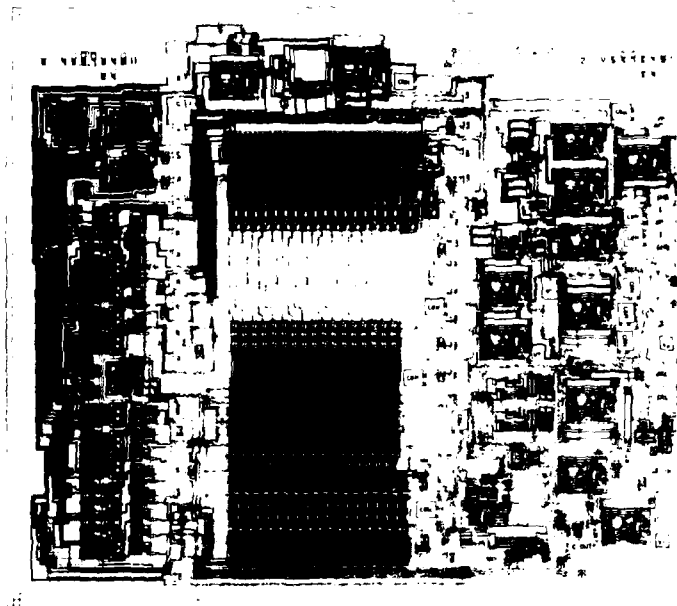


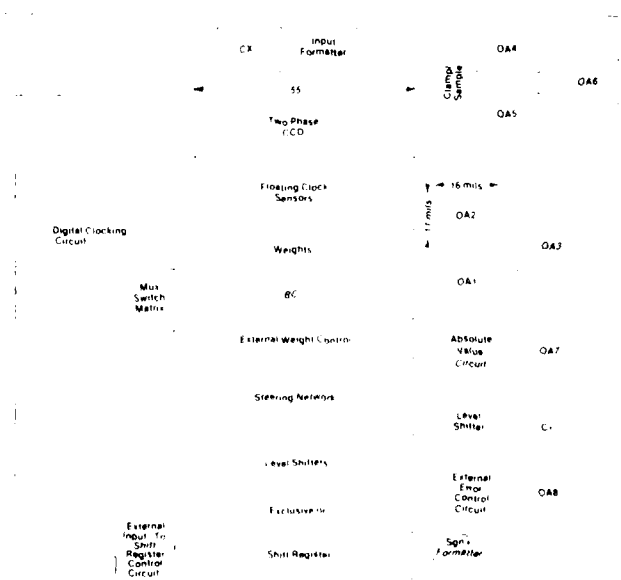
Figure 40b. Side View of CCD Analog Delay Line With Coplanar Overlapping Polysilicon Electrodes (Overlap = 2 μm)

A Cal-Comp plot of the CCD Adaptive Signal Processor is illustrated in figure 41. Bonding pads are strategically placed on the chip to evaluate intermediate operating points. The waveforms obtained on the various component sections of the CCD Adaptive Signal Processor and discussed in Section III, were obtained by either probing or bonding to these pads. For example, the CCD Analog Delay Line waveforms were obtained by examination of the tapped outputs as indicated in the center of figure 41. The organization of the chip is illustrated in figure 42. The digital clocking and waveform generation circuitry is located on the left side of the chip, whereas, all analog signal processing is maintained on the right side of the chip to minimize interaction. A more detailed description of the chip can be found in Section III and figure 8 which illustrates a complete schematic



80 0976 V 34

Figure 41. Cal-Comp Plot of the CCD Adaptive Signal Processor Integrated Circuit



80 0976 V 35

Figure 42. CCD Adaptive Signal Processor Chip Organization

of the functional operation. Figure 43 is a photomicrograph of the completed CCD Adaptive Signal Processor Integrated Circuit which is a 180 mil x 220 mil die size. The total power dissipation of the chip is approximately 250 mw and the frequency response limitation (i.e., sampling clock frequency of the CCD) is set by the bandwidth of the Operational Amplifiers which determines the settling time accuracy in the analog signal processor. Maximum CCD clocking frequency is about 100 kHz while minimum clocking frequency, set by thermal leakage considerations, is approximately 1 kHz.

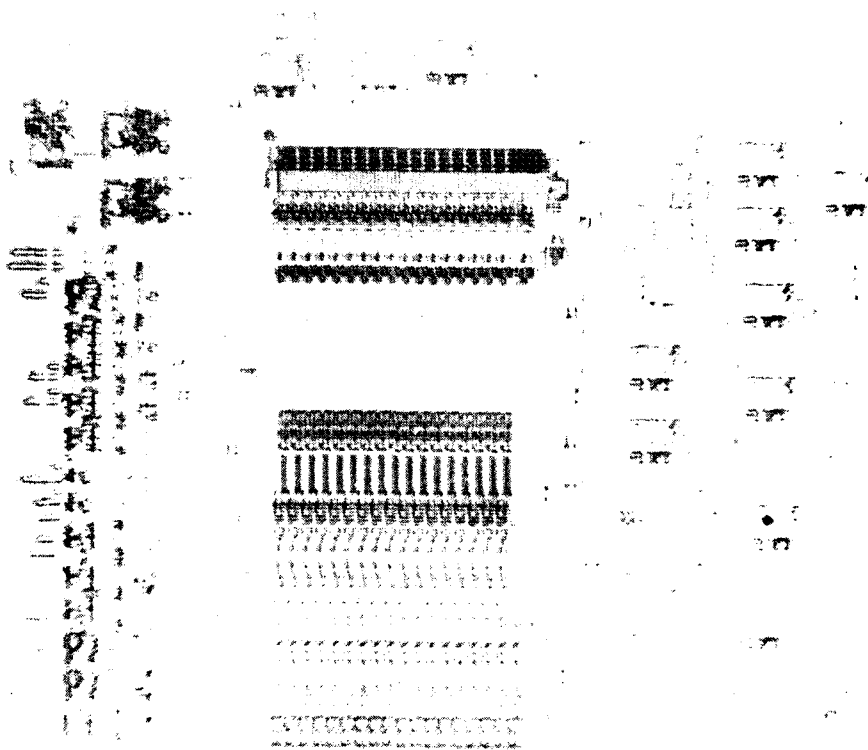


Figure 43. CCD Adaptive Signal Processor Photomicrograph
Chip Size 180 Mils x 220 Mils

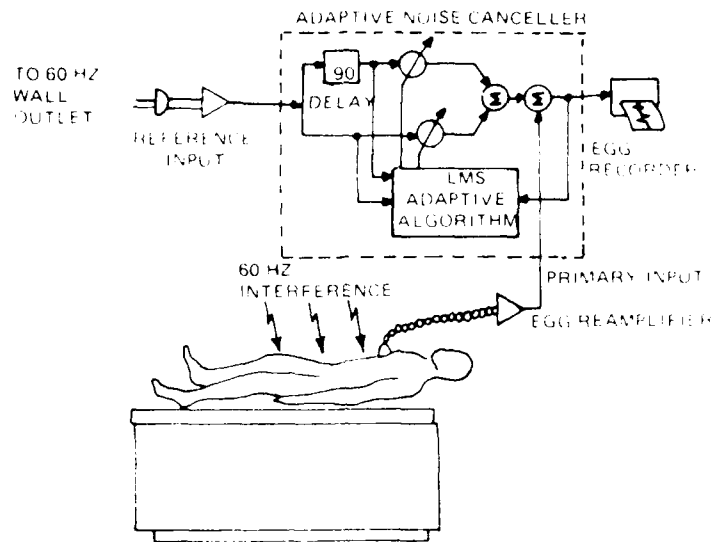
V. APPLICATIONS

There are a number of applications for adaptive filters with special need for real-time signal processing. Several applications are:

- Estimation/Predication
- Filtering
- Spectral Analysis
- Data Compression
- Interpolation
- Multiple Linear Regression
- Echo Cancellation
- Speech Analysis
- Noise Cancellation
- Coherent Signal Processing
- Frequency Measurement
- System Modeling

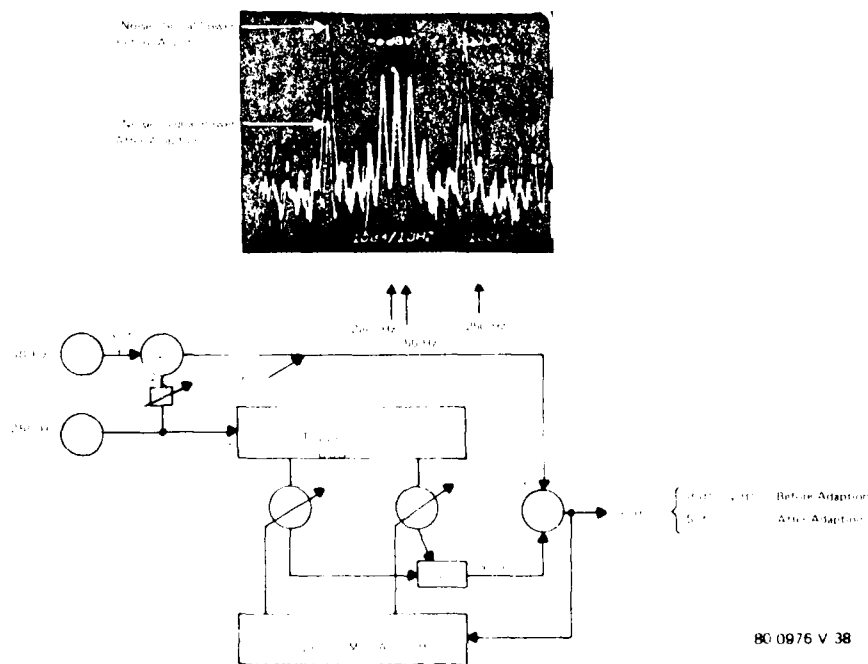
ADAPTIVE NOISE CANCELLATION

A very important application area is adaptive noise cancelling such as the removal of interference in electrocardiography, noise in speech signals, clutter cancellation in antenna (or similar type systems with hydrophones, seismic/acoustic transducers, electro-optical sensors, etc.) sidelobe interference, and coherent signal processing when periodic signals must be separated from broadband interference such as spread-spectrum systems. Figure 44 illustrates the application of adaptive noise cancelling to electrocardiography, such as cancellation of 60 Hz interference in conventional ECG, the donor ECG in heart transplants, and the maternal ECG in fetal electrocardiography. The advantage of this technique is the cancellation of the interference even when the latter drifts, since the reference input to the filter will also drift. An example of this application is illustrated in figure 45 which indicates the operation of the CCD Adaptive Filter before and after adaptation.



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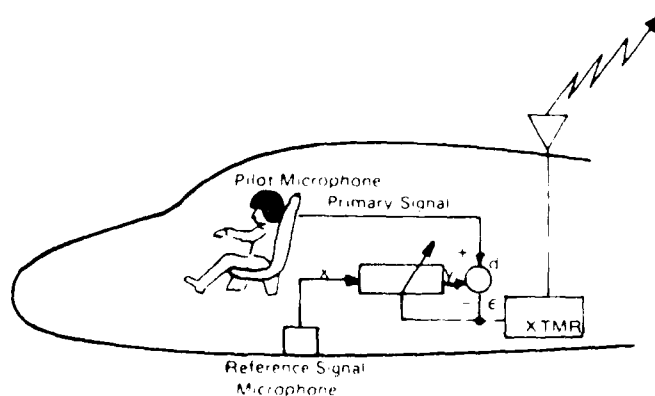
Figure 44. 60 Hz Interference Cancellation with a 2-Tap Adaptive Filter in Electrocardiography¹



80-0976-V-38

Figure 45. CCD Adaptive Noise Canceller With 2-Tap Adaptive Element

A second area is the cancellation of noise in speech signals such as the situation which arises in pilot communications with a high level of background engine noise. This interference contains strong periodic components in the speech frequency band and the intelligibility of the radio transmission is affected. A conventional filter would not be sufficient since the frequency and intensity of these interference signals vary with engine speed and load, in addition to the location of the pilots head. Figure 46 illustrates the cancellation of noise in this particular example. A reference input is obtained by placing a second microphone at a suitable location in the pilot's cabin. Experiments have performed¹ to illustrate the concept of noise cancellation with strong acoustical interference in speech transmission. The interference consisted of an audio frequency triangular wave that contained many harmonics which varied in amplitude and phase because of the multipath scattering effects throughout the room. Typically, 16 analog weights rendered the interference barely perceptible to the remote listener.



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Figure 46. Cancellation of Noise in Speech Communication

¹ B. Widrow, et. al., "Adaptive Noise Cancelling: Principles and Applications" Proc. IEEE 63, 1692 (1975).

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A CCD MONOLITHIC LMS ADAPTIVE ANALOG SIGNAL PROCESSOR INTEGRATE--ETC(U)
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A third area of noise cancelling is in adaptive cancellation of sidelobe interference in receiving arrays. For example, a sensor beamformer may be constrained with the adaptive noise canceller as shown in figure 47. The reference input to the noise canceller is obtained from the "organ-pipe" beam-former array after summation. Figure 48 illustrates photomicrographs of 16 and 69 input "organ-pipe" geometries² which buried channel CCD technology and on-chip, support circuits to reconstruct the sample-data signals.

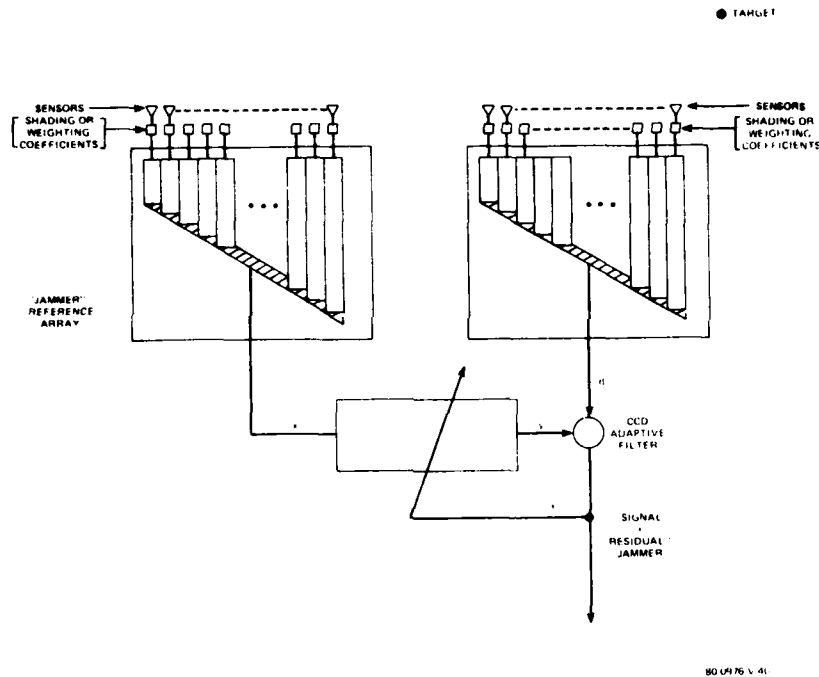
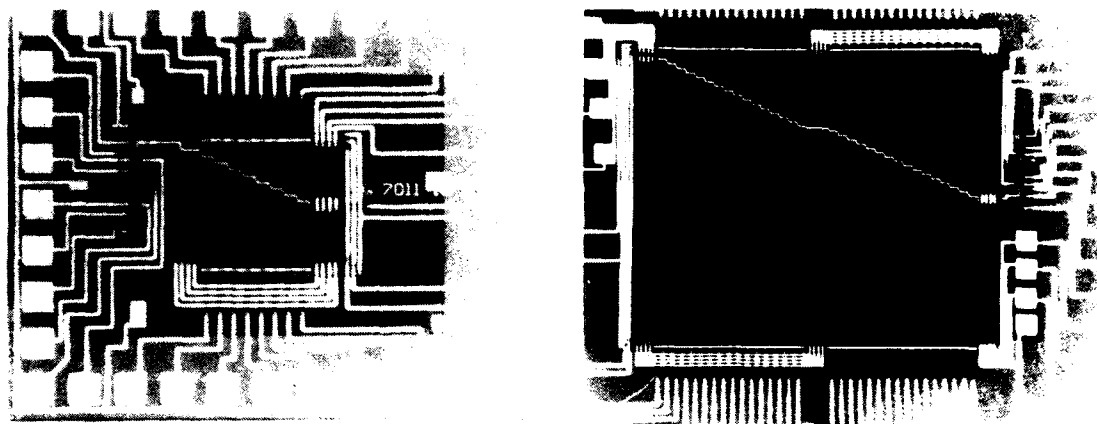


Figure 47. An Adaptive Beamformer Array to Remove Jammer Interference

¹B. Widrow, et. al., "Adaptive Noise Cancelling: Principles and Applications" Proc. IEEE 63, 1692 (1975)

²K.J. Petrosky and M.H. White, "CCD Sonar Beam-Forming". Proceedings of 1978 Conference on CCD Applications, San Diego, California.

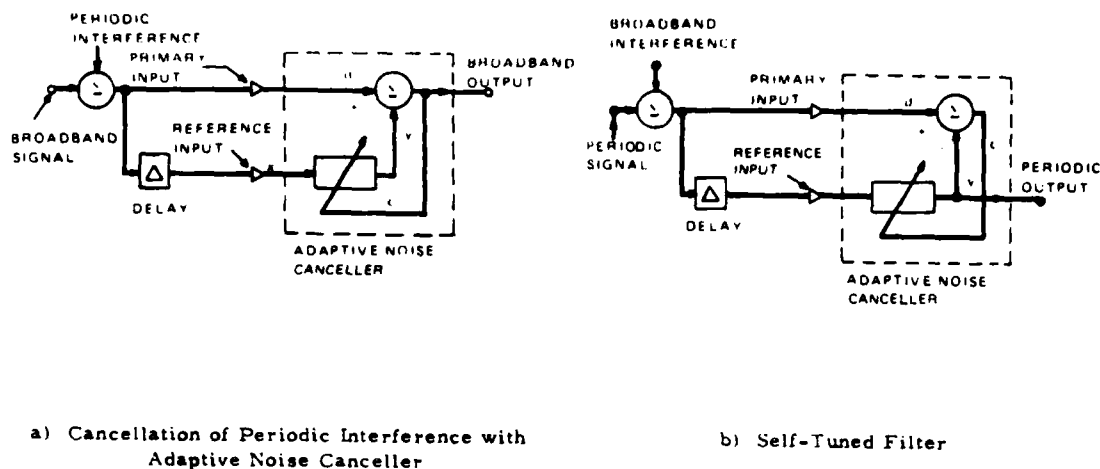


a) 16-Element Beamformer

b) 64-Element Beamformer

Figure 48. Photomicrograph of CCD Beamformer Devices

A fourth area of interest is the separation of broadband and periodic signals as illustrated in figure 49. The insertion of a fixed delay in the reference path, as shown in figure 49a decorrelates the broadband components and the narrow-band components remain correlated. This is an excellent method in the case when no external reference input is available such as speech or music playback in the presence of tape hum or turntable rumble. Another area of application is in spread-spectrum communication with narrow-band jamming. Figure 49b illustrates the recovery of the periodic components with applications to automatic signal seeking and the enhancement of low level sinusoidal signals buried in broadband noise. Thus, the adaptive filter functions as a coherent signal processor. An important application area is the use of the CCD Adaptive Signal Processor as a Maximum-Entropy Method (MEM) for a pre-whitening, clutter cancellation filter in Radar and Sonar Doppler Signal Processing.



80-0976-V-42

Figure 49. Separation of Broadband and Periodic Signals as in Spread Spectrum Systems

ADAPTIVE LINEAR PREDICTION FOR NARROWBAND SPEECH/VOICE PROCESSING

A promising area for CCD adaptive filtering is in speech processing where redundancy in the spoken word has long been recognized by researchers. Electrical processing of speech which takes into account this redundancy can be used to substantially reduce the bandwidth required for speech transmission. For example, if speech is sampled and quantized at 56 k bits/sec (7 bits or 128 possible amplitude levels per sample at 8 k samples/sec) for acceptable fidelity and the channel bandwidth restricts transmission to below 4 k bits/sec, then a speech compression ratio of approximately 15:1 is attempted. This low data rate would permit speech to be transmitted over high frequency radio or telephone links which have bandwidths barely wide enough for the original analog speech sounds. Such a narrow-band voice digitizer may be used in frequency division multiplexing for simultaneous transmission over wide-band channels. Narrow-band digitized speech

lends itself to encryption for secure communications and provides a better S/N than a wide-band digitizer particularly in RF transmission communication satellite links with limited or fixed available power.

"Speech compression, which maintains intelligibility, has always been difficult because speech consists of more than words and messages. Speech has the vocal timbre and conversational idiosyncrosies of the speaker and the emotion behind his words. It is normally constructed in an imprompt manner and delivered in a free and informal fashion. Speech flows in time as a continuation that a voice digitizer must process in real time, leaving no chance for later evaluation or correction. Although the information content of the message itself may be low, (possibly below 100 bits/sec), transmission of the subtle vocal inflections requires a data rate of several thousand bits/sec."³ Historically, speech compression and reconstruction began with the Dudley channel vocoder in 1936 in which the Fourier Spectrum characteristics of speech determined the parameters of a filter bank. This vocal tract filter bank approximated the vocal tract resonance characteristics of speech and it was excited by a pulse generator (variable period) to approximate the vowels or larynx vibration and a random noise generator to represent the consonants or fricative nasal sounds.

Another technique has proven quite successful in speech compression: linear predictive analysis.⁴ The Fourier analysis method treats the past signal, and the linear predictive analysis method attempts to predict the future signal. Linear prediction uses time domain characteristics of the speech signal and the voice signal is analyzed as a linear combination of present and past values to form a set of prediction coefficients. If 10 to 12

³G.S. Kang, "Linear Productive Narrowband Voice Digitizer" EASCON 74, 51, Washington, D.C. Oct. 7-9, 1974.

⁴B.S. Atal and S.L. Hanauer. "Speech Analysis and Synthesis by Linear Prediction of the Speech Wave", J. of Acoust. Soc. Amer., 50, 637 (1971).

consecutive samples of speech are taken (i.e., a speech segment of 1.25 to 1.5 milliseconds), then prediction coefficients can be generated as the tap weights in an adaptive filter. Although only 10 to 12 prediction coefficients are needed, one must accumulate many speech samples (e.g., 100 to 200 samples) to determine these coefficients with some degree of accuracy. The accuracy of these measurements was discussed by Gauss, with regards to highly redundant or over-determined equations, and he formulated the method of least-squares. This method is used in the CCD adaptive filter.

Figure 50 illustrates a functional diagram of a conventional digital linear productive narrowband voice processor. The major functional elements of this system are

- vocal tract analyzer
- pitch extractor
- voice/unvoice analyzer
- encoder/decoder
- synthesizer

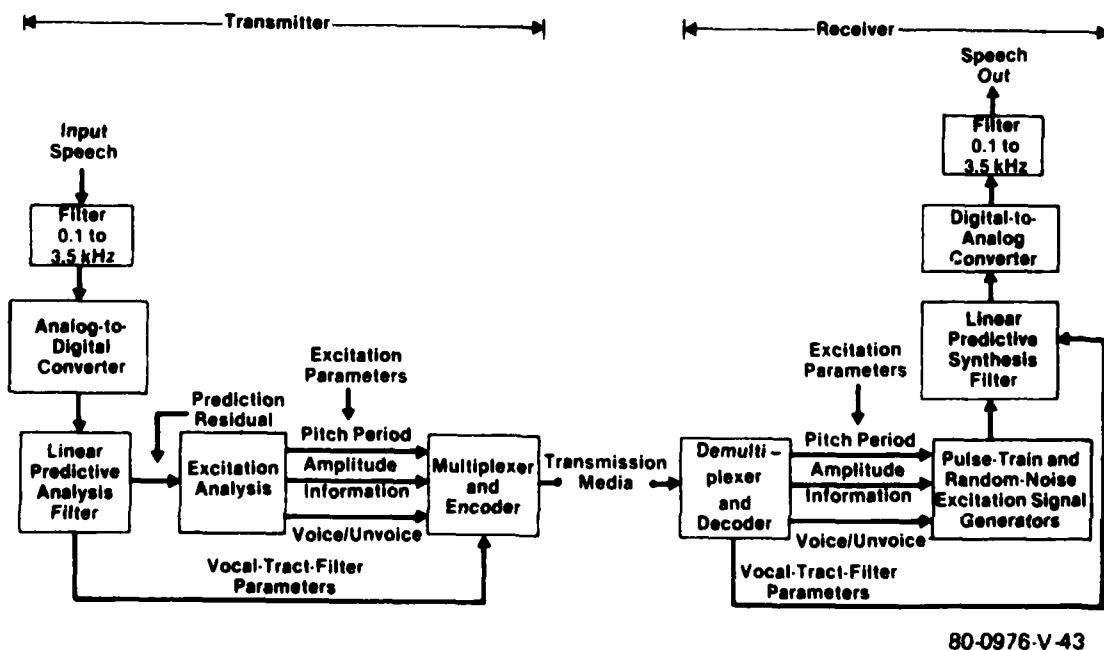


Figure 50. Narrowband Voice System

Digital systems which use linear prediction have been analyzed and built,^{5,6} however, the major limitations to an all digital approach are size, power dissipation, and cost. Table 8 illustrates a comparison between the digital, hybrid, and discrete analog sampled approaches for a narrow-band voice system.

Figure 51 illustrates the use of the CCD Adaptive filter as an Analysis filter to generate the prediction coefficients $W_1 \dots W_N$. The voice input is band-pass filtered and inputted to the adaptive filter. The filter input is also used as the primary or desired signal to generate an error called the prediction residual. This error may be further messaged to extract the pitch period, amplitude, and voice/unvoice decision. The speech sample may be nominally 20 msec in length and the error must converge to its minimum value in this time frame. Near the end of the time frame, a unit pulse is inserted into the filter and the filter output becomes the converged weights or prediction coefficients. The clipped data LMS algorithm has been computer/simulated at NRL⁷ with the following constraints,

- preemphasis filter on the input signal
- $W_k \leq 0.98$
- an increase of the unit circle (Z-domain) by 10 percent with scaling of the prediction coefficients
- 10 prediction coefficients of bit levels: 8,8,8,8,7,7,7,6,5,5
- data rate of 3600 bits/sec.

The prediction coefficients generated with the clipped data LMS algorithm and the above constraints were used to synthesize speech. Test sentences were employed and the playback of the reconstructed speech indicated good speech reproduction and quality, although the

⁵J.E. Dunn, J.R. Lowan and A.J. Russo, "Progress in The Development of a Digital Vocoder Employing on Itakura Adaptive Predictor" (1973)

⁶Final Report, Voice Processor LSI/Organization Optimization Study, Contract No. DCA 100-75-C-0020, Sept. 1975 TRW Systems Group, Redondo Beach, Cal.

⁷G.S. Kang, Private Communication, Naval Research Laboratories (1977)

TABLE 8
NARROWBAND VOICE DIGITIZER

	# of I. C. 's	Power	Size	Prod. Cost	Risk
Digital	125	50w	3"x5"x12"	10k	Low
Hybrid	40	-	3"x5"x6"	-	Med
DASP	12	7w	1"x5"x5"	0.5-1k	High

80-0976-V-45

latter is a subjective parameter. Thus, a CCD adaptive filter with 10 weights operating at a 8 kHz xample rate is an excellent candidate for this particular application.

Robust Linear predictive coding (LPC) Systems required a "prewhitening" type filler preceding the analyzer to remove strong narrow-band interference. The CCD Adaptive Signal Processor may be used as (1) a front-end noise-canceller preceding the (2) analyzer portion of the LPC system.

ADAPTIVE ECHO CANCELLATION FILTERS

An important application of CCD adaptive transversal filters is in echo cancellation in the telephone network.⁸ Weinstein says, "It is, to be honest, remarkable that a technique (echo cancellation) which has been studied, favorably appraised, and implemented

⁸S.B. Weinstein, "Echo Cancellation in the Telephone Network", IEEE Communications Society Magazine, pg. 9, Jan. 1977.

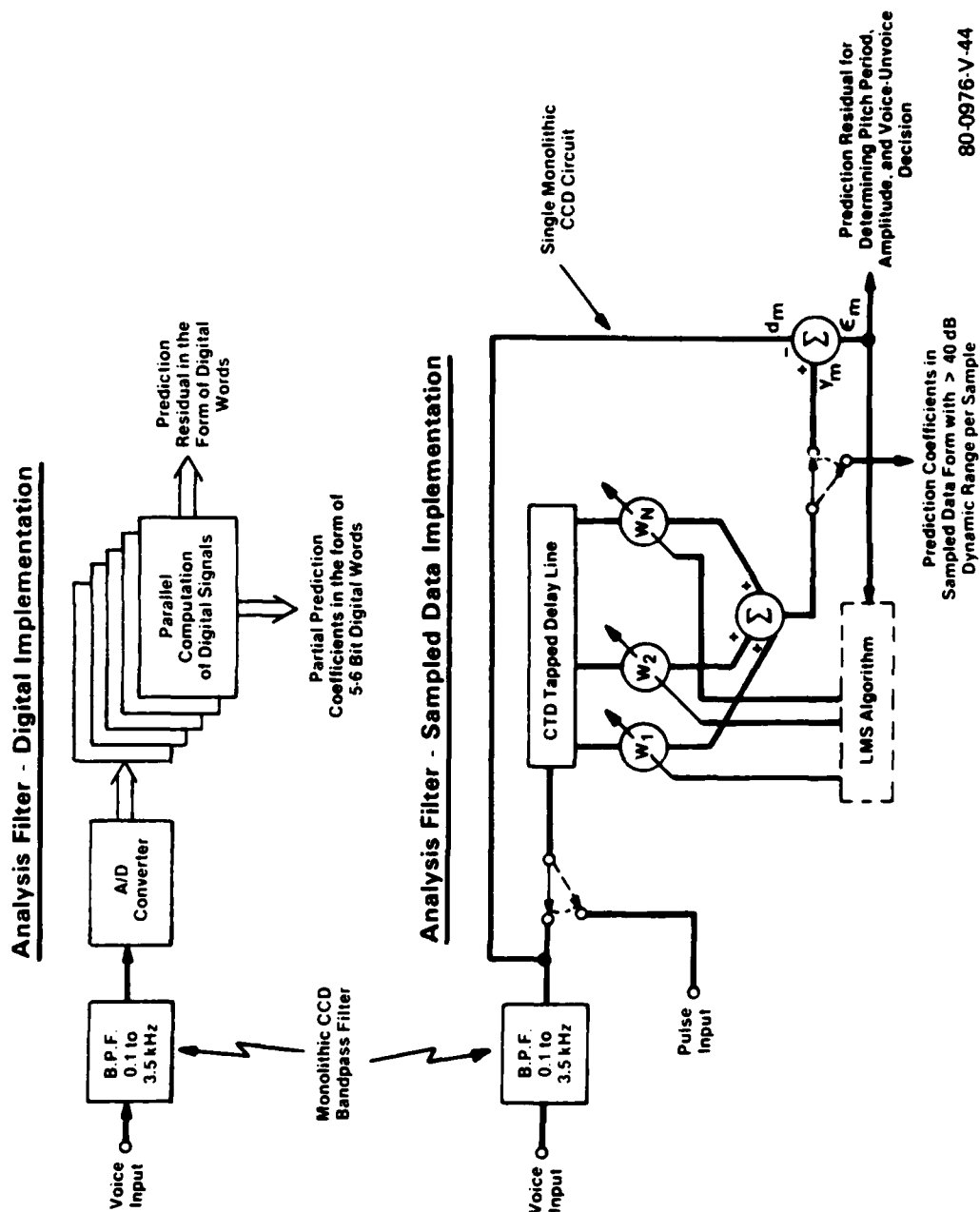


Figure 51. CCD Adaptive Filter for Linear Prediction Analysis of Speech

in experimental hardware for more than 10 years has still not been commercially applied. The obvious reason is that echo cancellers which performs better than echo suppressors have tended to cost much more than echo suppressors, it is intrinsically more difficult to discover and separate an echo from a mixture of signals than to block everything." CCD adaptive filters offer a means to realize such an echo canceller.

The study of echos in the telephone network has shown that it is difficult to conduct a conversation when a person's voice returns with a delay greater than a few tens of milliseconds. The long-delayed echos are irritating and returns attenuated -40 dB below the speakers voice level will cause the speaker problems. Echos occur due to impedance mismatches in the communication system as illustrated in figure 52a, which describes signal leakage and reflection at the hybrid coupler. Figure 52b illustrates how an echo canceller is used to model the echo channel and generate an output echo replica to cancel the echo. This is particularly important in satellite-routed circuits which experience signal delays in excess of 500 msec. Digital echo-canceller chips have been built⁹ to interface with either an 8-bit μ -law or A-law code for CODEC Applications.

SYSTEM MODELING

Perhaps one of the most important future applications of a monolithic adaptive CCD adaptive signal processor is system modeling. In this instance, an unknown system whose system transfer function is changing with time is to be measured in real time and in response to specific system inputs. Paralleling the unknown system with a CCD adaptive signal processor, the process of minimizing the MSE provides a set of adaptive processor weights which represent the impulse response (transfer function) of the system to be modeled. Once the impulse response is determined,

⁹D.J. Duttweiler, "Bell's Echo-Killer Chip" IEEE Spectrum, 17, 34 (1980).

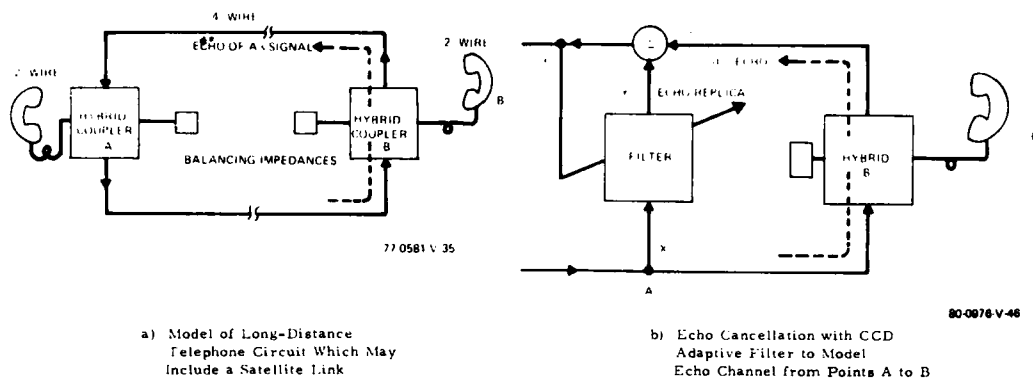


Figure 52. Echo Cancellation With CCD Adaptive Filters

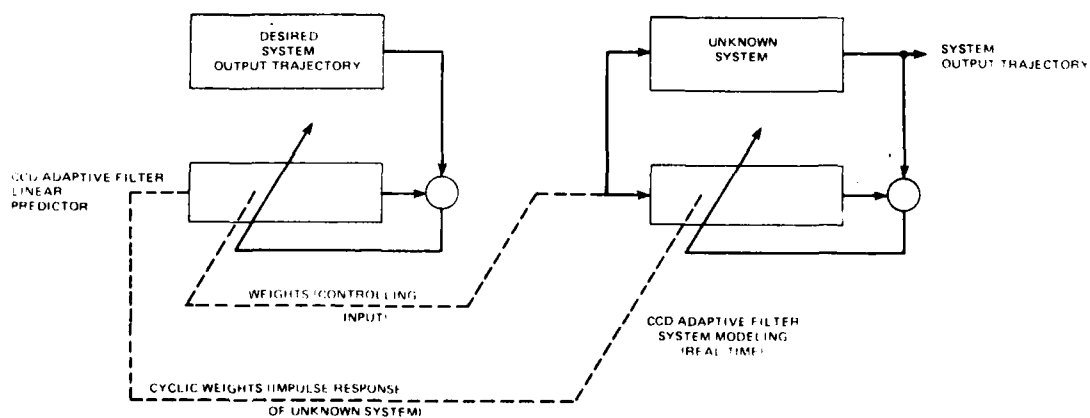
the response of the system to another input is known. In particular, if a certain system output response is desired, then the system input can be adjusted in real time to provide this output response. Figure 53 illustrates the concept of system modeling as applied to adaptive predictive control. The unknown system is modeled in real-time, while in compressed time (off-line) the predicted control inputs to the system are determined with the CCD Adaptive Filter employed as a linear predictor.¹⁰ The use of adaptive predictive control (APC) has been the subject of many papers in the literature, particularly, the work of Richalet.¹¹ APC may be applied in a number of application areas as illustrated in table 9. A particular area of interest is in the control of

¹⁰G. Axelby, Private Communication, Westinghouse Electric Corp.

¹¹J. Richalet, et. al, "Model Predictive Heuristic Control: Applications to Industrial Processes", Automatica, Pergamon Press (1978).

TABLE 9
APPLICATIONS

- | | |
|---|---|
| <ul style="list-style-type: none"> • Machine Tool Systems • Robotics • Process Control • Electrical Power Generation • Jet Engine Control • Nuclear Power Plant Control • Ignition, Water/Heat, and Exhaust Control in Automobiles | <ul style="list-style-type: none"> • Manufacturing Processes • Maritime Controls For Ships • Missile and Aircraft • Waste Water Purification and Desalination • Biological Control Systems |
|---|---|



80-0976 V.4.7

Figure 53. System Modeling as Applied to Adaptive Predictive Control

industrial robots, where high speed operation will be required in the future.¹² For example, in the case of an industrial robot for machining functions there are (1) cutting depth and feed-rate controls required when the grinding force varies, (2) changes relating to the location or orientation of a part within the robots area of influence may be controlled with tactile (e.g., pressure) and visual sensors which provide inputs to adapt to a changing environment. Table 10 illustrates the features that APC can provide for Industrial Robotics.

TABLE 10
INDUSTRIAL ROBOTICS

- Built-In Electronic Intelligence
- No Speed Change Gears or Belts
- No Brakes or Limit Switches
- Rapid Movement
- Accuracy
- Repeatability

¹²"Busy Robots Spur Productivity" IEEE Spectrum, Sept. 1979, pg 31-36.

VI. CONCLUSIONS

For the first time, an entire 16-tap weight Adaptive Signal Processor, which employs the "clipped-data" LMS Error Algorithm, has been implemented on a monolithic silicon chip of 180 mils x 220 mils die size. The inputs to the chip are analog and the processor uses discrete analog signal processing (DASP) to achieve a dynamic range of 60 dB in analog signal processing, a 50-dB dynamic range in the weights, and a maximum sampling frequency of 100 KHz. The organization of the Adaptive Signal Processor is a simultaneous up-date of the weights for each data sample entry into the processor, where the error is determined on a sample-to-sample basis. The entire power dissipation is approximately 200 mW and is determined by the operational amplifiers and comparators which set the sampling rate by the settling times in the sampling circuitry. The technology is CMOS bulk with double polysilicon electrodes of 7 μ m lines and 5 μ m spacings to achieve 2-1/2 phase CCD (surface channel) operation with non-destructive tapping of the analog signal samples. The CMOS technology permits the realization of analog operational amplifiers (11 mils x 16 mils) and comparators, together with CMOS logic, buffer I/O's, and level translator-drivers.

A comparison of the DASP approach for advanced adaptive signal processing with the conventional digital implementation indicates the advantages for the former. The digital approach would have to achieve a minimum 8-bit resolution in signal and tap weight dynamic range to be comparable to DASP. An analysis of the digital implementation indicates the need for a 16K gate chip (gate = 2-input NAND gate) custom layout, minimum feature sizes of 2 μ m (i.e., 2 μ m lines and spacings), double

metal technology, and CMOS bulk technology for low standby power dissipation. In addition, 2 A/D converters and 2 D/A converters would be required to provide the necessary I/O capability of the DASP implementation of the Adaptive Signal Processor. The digital portion of the processor (i.e., the 16K gate chip) is in keeping with the goals of VHSIC, phase 1, where a functional throughput rate (FTR) = 5×10^{11} is desired. In this example, a 16K gate chip of 250 mils x 250 mils die size, and operating at a 20 MHz clock rate (this rate is required to access signal and weight data from RAM and to achieve the 8 x 8 digital multiples for a nominal 50 KHz sampling rate) would provide a FTR = 7.8×10^{11} gates-cm⁻²Hz (e.g., 16K x 20 MHz/(0.4 cm²)). Although the advantages of the digital approach are the extremely slow sampling rates for control applications, and the storage and retrieval of weight values for system modeling, etc., the cost and yield of such a chip, exclusive of the power dissipation and A/D - D/A requirements, are certain to be easily an order of magnitude over the DASP approach.

In this preliminary study of the feasibility of DASP for such an Adaptive Signal Processor we concentrated on the system architecture and technology which would lead to a monolithic silicon chip, and would be extendible to other architectures and algorithms, and permit the increase in tap weights from an initial value of 16 to say, 256. The basic components of the Adaptive Signal Processor are the CCD Analog Delay Line with non-destructive taps, a set of adjustable tap weights represented by the electrically reprogrammable analog conductance MOSFET's and an algorithm, to control and up-date the weights. The Adaptive Signal Processor has been designed with versatility in mind. Internally or externally generated errors may be used to adjust the tap weights at each tap location. In addition, the weight values may be determined internally or programmed externally from MDAC's. A feature exists to recycle the weights for long retention. A so-called "bias-tap" or 17th tap is employed to measure the average level of the incoming reference signal

and may be used to compensate for input drift. A provision exists for the cascading of chips to achieve longer chains of tap weights. Finally, the control of the convergence and accuracy of the adaptive signal processor is accomplished with an off-chip scaling network.

The basic functional components of the Adaptive Signal Processor chip have been evaluated as described in this report. Minor photographic mask modifications have been made to correct the few errors in circuit layout and selection of component values. Additional processing and evaluation is planned to permit the complete evaluation of the Adaptive Signal Processor. The applications of this type of Adaptive Signal Processor are wide-ranging and should have a large impact on the development of advanced VLSI signal processing systems.

APPENDIX A

The simplified block diagram of the adaptive filter shown in figure A-1 is used to calculate the convergence factor. For a given tap output, x_k , the weighted output voltage, $v_o(m)$, is given by

$$v_o(m) = R (g_{ds}^+(m) - g_{ds}^-(m)) x_k(m)$$

which yields an effective weight

$$\begin{aligned} W_k(m) &= v_o(m) / x_k(m) \\ &= R (g_{ds}^+(m) - g_{ds}^-(m)) \end{aligned}$$

where:

$$\begin{aligned} g_{ds}^+(m) &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gw}^+(m) - V_T) \\ &= \beta (V_{GW}^+(m) - V_T) \end{aligned}$$

$$g_{ds}^-(m) = \beta (V_{GW}^-(m) - V_T)$$

Referring to the figure

$$g_{ds}^+(m+1) = \beta \left[V_{GW}^+(m) + G_\epsilon G_{BC^3} |\epsilon| - V_T \right]$$

where:

$$\begin{aligned} G_\epsilon &\triangleq \text{error channel gain} \\ &= R_{ext} R \text{ (see figure A-1)} \end{aligned}$$

$$\begin{aligned} G_{BC^3} &= \text{gain of } BC^3 \text{ circuit} \\ &= \frac{C_2}{C_g} \text{ (see figure A-1)} \end{aligned}$$

$$\begin{aligned}
 \therefore W_k(m+1) &= [g_{ds}^+(m+1) - g_{ds}^-(m+1)] R \\
 &= W_k(m) + \beta R G_{\epsilon} G_{BC3} |\epsilon| \\
 &= W_k(m) + 2 \mu |\epsilon|
 \end{aligned}$$

$$\begin{aligned}
 \therefore \mu &= \frac{\beta R G_{\epsilon} G_{BC3}}{2} \\
 &= \frac{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} R \frac{R_{ext}}{R} \frac{C_2}{C_g}}{2}
 \end{aligned}$$

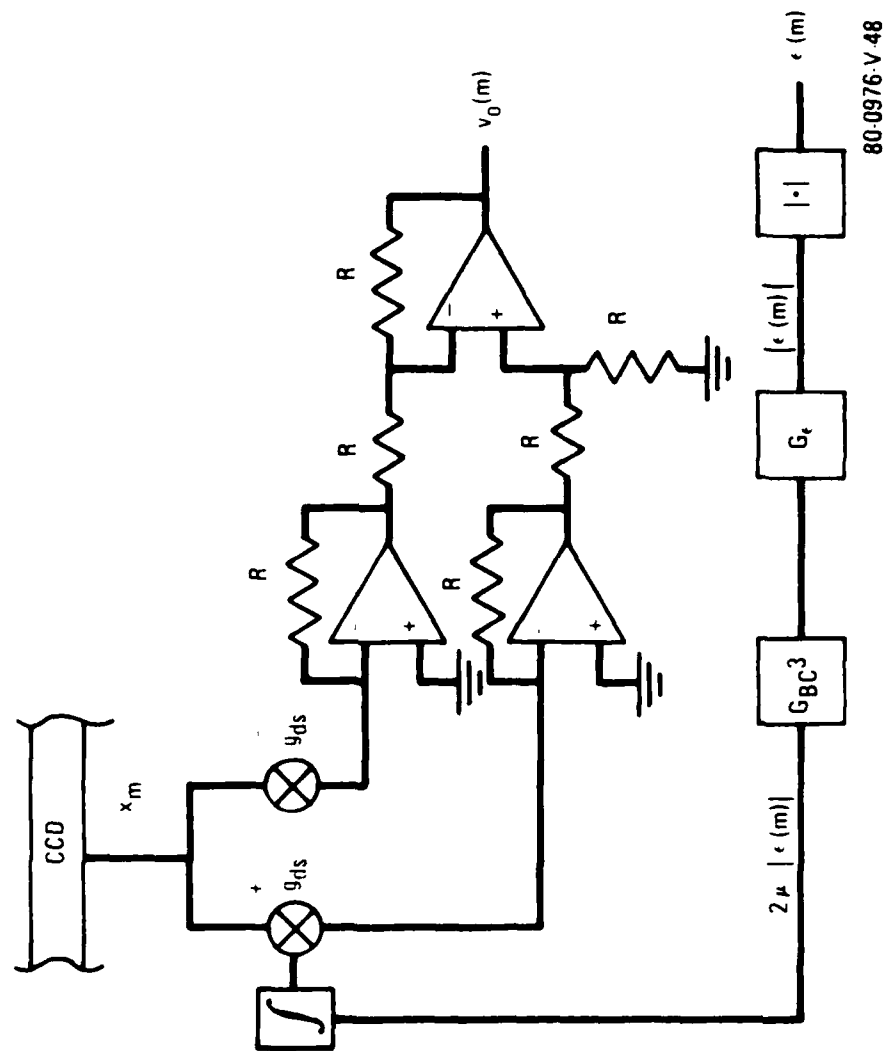
$$\mu_n = 550 \text{ cm}^2/\text{V sec}$$

$$C_{ox} = 3.4 \times 10^{-8} \text{ f/cm}^2$$

$$\frac{W}{L} = 2$$

$$\frac{C_2}{C_g} = 5$$

$$\therefore \mu = (4.68 \times 10^{-5}) R_{ext}$$



80-0976-V-48

Figure A-1. Adaptive Filter Block Diagram